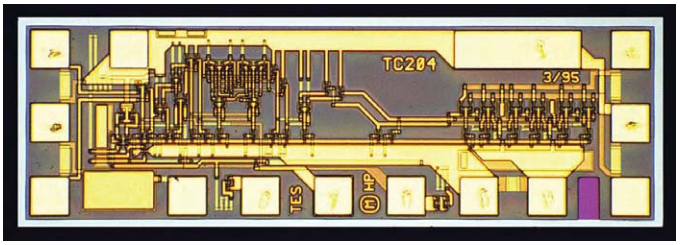
Agilent HMMC–3002
DC–16 GHz GaAs HBT MMIC
Divide–by–2 Prescaler

1GC1-8004

Data Sheet



Chip Size: 1330 x 440 µm (52.4 x 17.3 mils)
Chip Size Tolerance: ± 10 µm (± 0.4 mils)
Chip Thickness: 127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions: 70 x 70 µm (2.8 x 2.8 mils)

Features

- **Wide Frequency Range: 0.2-16 GHz**
- **High Input Power Sensitivity: On–chip pre– and post–amps -20 to +10 dBm (1–10 GHz) -15 to +10 dBm (10–12 GHz) -10 to +5 dBm (12–15 GHz)**
- **Dual–mode P_{out}: (Chip Form) +6.0 dBm (0.99 Vp–p) @ 80 mA 0 dBm (0.5 Vp–p) @ 60 mA**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range: 4.5 to 6.5 volt operating range**
- **Differential I/O with on–chip 50 Ω matching**

Description

The HMMC-3002 GaAs HBT MMIC Prescaler offers dc to 16 GHz frequency translation for use in communications and EW systems incorporating high–frequency PLL oscillator circuits and signal– path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise. In addition to the features listed above the device offers an input disable contact pad to eliminate any self–oscillation condition.

Absolute Maximum Ratings[1]

(T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply Voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
$V_{Disable}$	Pre-amp disable voltage	V_{EE}	V_{CC}	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damge to the device.
2. MTTF > 1 x 10^6 hours @ $T_{BS} \leq 85°C$. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

Agilent Technologies

dc Specifications/Physical Properties[1]

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current (**HIGH** Output Power Configuration[2]: $V_{PwrSel} = V_{EE}$)	68	80	92	mA
	Bias supply current (**LOW** Output Power Configuration: V_{PwrSel} = open)	51	60	69	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self–bias voltage, generated on–chip)	V_{CC} -1.45	V_{CC} -1.35	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified suply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.
2. High output power configuration: P_{out} = +6.0 dBm (V_{out} = 0.99 V_{p-p}). Low output power configuration: P_{out} = 0 dBm (V_{out} = 0.5 V_{p-p}).

RF Specifications

(T_A = 25°C, Z_0 = 50Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	16	18		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self–Osc.}$	Output Self–Oscillation Frequency[2]		6.8		GHz
P_{in}	@ dc, (Square–wave input)	-15	≥ 25	+10	dBm
	f_{in} = 500 MHz, (Sine–wave input)	-15	≥ 20	+10	dBm
	f_{in} = 1 to 10 GHz	-15	≥ 25	+10	dBm
	f_{in} = 10 to 12 GHz	-10	≥ 15	+10	dBm
	f_{in} = 12 to 15 GHz	-4	≥ 10	+4	dBm
RL	Small–Signal Input/Output Return Loss (@f_{in} < 12 GHz)		15		dB
S_{12}	Small–Signal Reverse Isolation (@f_{in} < 12 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a (f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero–crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output Edge speed (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave input signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Pre-amp Disable ($V_{Disable}$) feature, or the Differential Input de-biasing technique.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	High Output Power Operating Mode[1] Min.	Typ.	Max.	Units
P_{out}	@ f_{out} < 1 GHz	4.0	6.0		dBM
	@ f_{out} = 2.5 GHz	3.5	5.5		dBm
	@ f_{out} = 5 GHz	2.0	4.0		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.79	0.99		volts
	@ f_{out} = 2.5 GHz	0.74	0.94		volts
	@ f_{out} = 5 GHz	0.63	0.79		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 12 GHz, Unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-48		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, Both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-68		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, Referred to $P_{in}(f_{in})$		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, Referred to P_{out} (f_{out}))		-25		dBc
		Low Output Power Operating Mode[2]			
P_{out}	@ f_{out} < 1 GHz	-2	0		dBm
	@ f_{out} = 2.5 GHz	-2.5	-0.5		dBm
	@ f_{out} = 5 GHz	-4.0	-2.0		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.39	0.5		volts
	@ f_{out} = 2.5 GHz	0.37	0.47		volts
	@ f_{out} = 5 GHz	0.31	0.39		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 12 GHz, Unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-57		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, Both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-77		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, Referred to $P_{in}(f_{in})$)		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, Referred to $P_{out}(f_{out})$)		-30		dBc

Notes

1. $V_{PwrSel} = V_{EE}$.
2. V_{PwrSel} = Open Circuit.

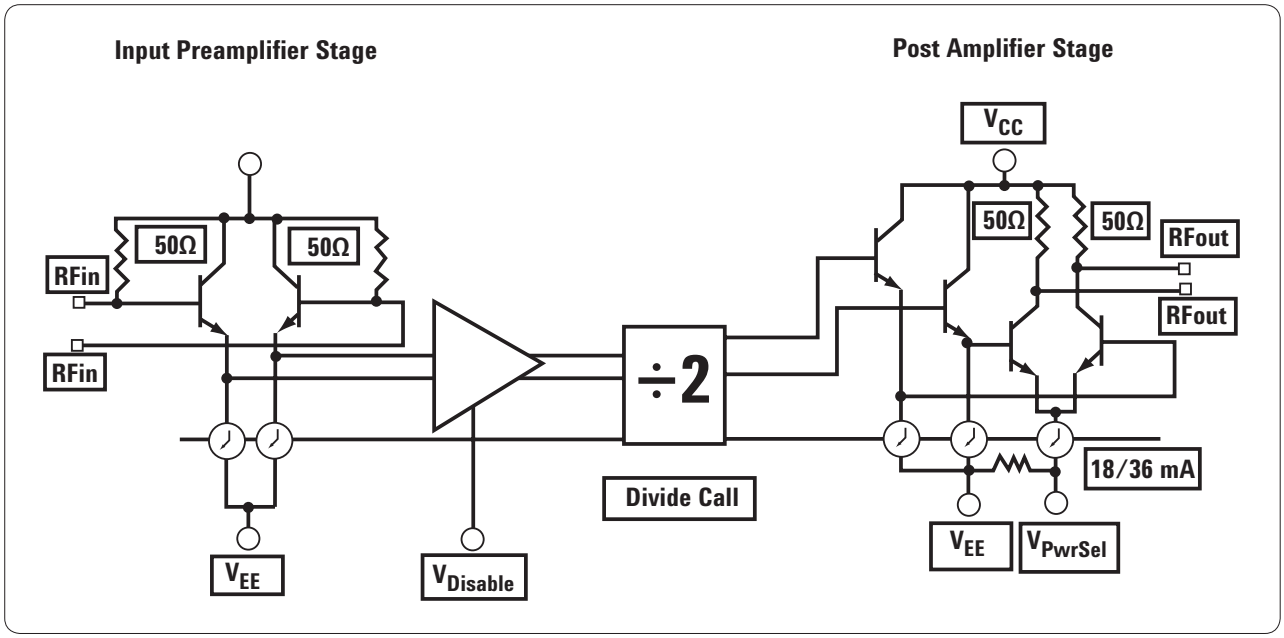


Figure 1. Simplified Schematic

Applications

The HMMC-3002 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase–noise PLL control circuitry or broad–band frequency translation is required.

Operation

The device is designed to operate when driven with either a single–ended or differential sinusoidal input signal over a 200 MHz to 16 GHz bandwidth. Below 200 MHz the prescaler input is "slew–rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square–wave.

The device may be biased from either a single positive or single negative supply bias. The backside of the device is not dc connected to any dc bias point on the device.

For positive supply operation V_{CC} is nominally biased at any voltage in the +4.5 to +6.5 volt range with V_{EE} (or V_{EE} & V_{PwrSel}) grounded. For negative bias operation V_{CC} is typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to V_{EE} (or V_{EE} & V_{PwrSel}).

Several features are designed into this prescaler:

1. Dual–Output Power Feature
Bonding both V_{EE} and V_{PwrSel} pads to either ground (positive bias mode) or the negative supply (negative bias mode), will deliver ~0 dBm [0.5 $V_{p–p}$] at the RF output port while drawing ~40 mA supply current. Eliminating the V_{PwrSel} connection results in reduced output -6.0 dBm [0.25 $V_{p–p}$] but at a reduced current draw of ~30 mA resulting in less overall power dissipation.

(NOTE: V_{EE} must ALWAYS be bonded and V_{PwrSel} must NEVER be biased to any potential other than V_{EE} or open–circuited.)

2. V_{Logic} ECL Contact Pad
Under normal conditions no connection or external bias is required to this pad and it is self–biased to the on–chip ECL logic threshold voltage (V_{CC} -1.35 V). The user can provide an external bias to this pad (1.5 to 1.2 volts less than V_{CC}) to force the prescaler to operate at a system generated logic threshold voltage.

3. Input Disable Feature
If an RF signal with sufficient signal–to–noise ratio is preent at the RF input, the prescaler will operate and provide a divided output equal to the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the device may "self–oscillate", especially under small signal input powers or with only noise present at the input. This "self–oscillation" will produce an undesired output signal also known as a false trigger. By applying an external bias to the input disable contact pad (more positive than V_{CC} - 1.35 V), the input preamplifier stage is locked into either logic *"high"* or logic *"low"* preventing frequency division and any self–oscillation frequency which may be present.

4. Input dc Offset
Another method used to prevent false triggers or self–oscillation conditions is to apply a 20 to 100 mV dc offset voltage between the RF_{in} and $\overline{RF}_{in}$ ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 kΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ~25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

Assembly Techniques

Figure 3 shows the chip assembly diagram for single–ended I/O operation through 12 GHz for either positive or negative bias supply operation. In either case the supply contact to the chip must be capacitively bypassed to provide good input sensitivity and low input power feedthrough. Independent of the bias applied to the device, the backside of the chip should always be connected to both a good RF ground plane and a good thermal heat sinking region on the mounting surface.

All RF ports are dc connected on–chip to the V_{CC} contact through on–chip 50 W resistors. Under any bias conditions where V_{CC} is not dc grounded, the RF ports should be ac coupled via series capacitors mounted on the thin–film substrate at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the device backside may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

All bonds between the device and this bypass capacitor should be as short as possible to limit the inductance. For operation at frequencies below 1 GHz, a large value capacitor must be added to provide proper RF bypassing.

Due to on–chip 50 Ω matching resistors at all four RF ports, no external termination is required on any unused RF port. However, improved *"Spitback"* performance (~20 dB) and input sensitivity can be achieved by terminating the unused RF_{out} port to V_{CC} through 50 Ω (positive supply) or to ground via a 50 Ω termination (negative supply operation).

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Optional dc Operating Values/Logic Levels[1]

(T_A = 25°C)

Function	Symbol	Conditions	Min (volts/mA)	Typical (volts/mA)	Max (volts/mA)
Logic Threshold[1]	V_{Logic}		V_{CC}-1.5	V_{CC}-1.35	V_{CC}-1.2
Input Disable	$V_{Disable(High)}$ [Disable]		V_{Logic} + 0.25	V_{Logic}	V_{CC}
Input Disable	$V_{Disable(Low)}$ [Enable]		V_{EE}	V_{Logic}	V_{Logic} - 0.25
Input Disable	$I_{Disable}$	$V_D > V_{EE}+3$	($V_{Disable}$ -V_{EE} - 3)/500	($V_{Disable}$ -V_{EE} -3)/500	($V_{Disable}$ -V_{EE} -3)/500
Input Disable	$I_{Disable}$	$V_D < V_{EE}+3$	0	0	0

Note:
1. Acceptable voltage range when applied from external source.

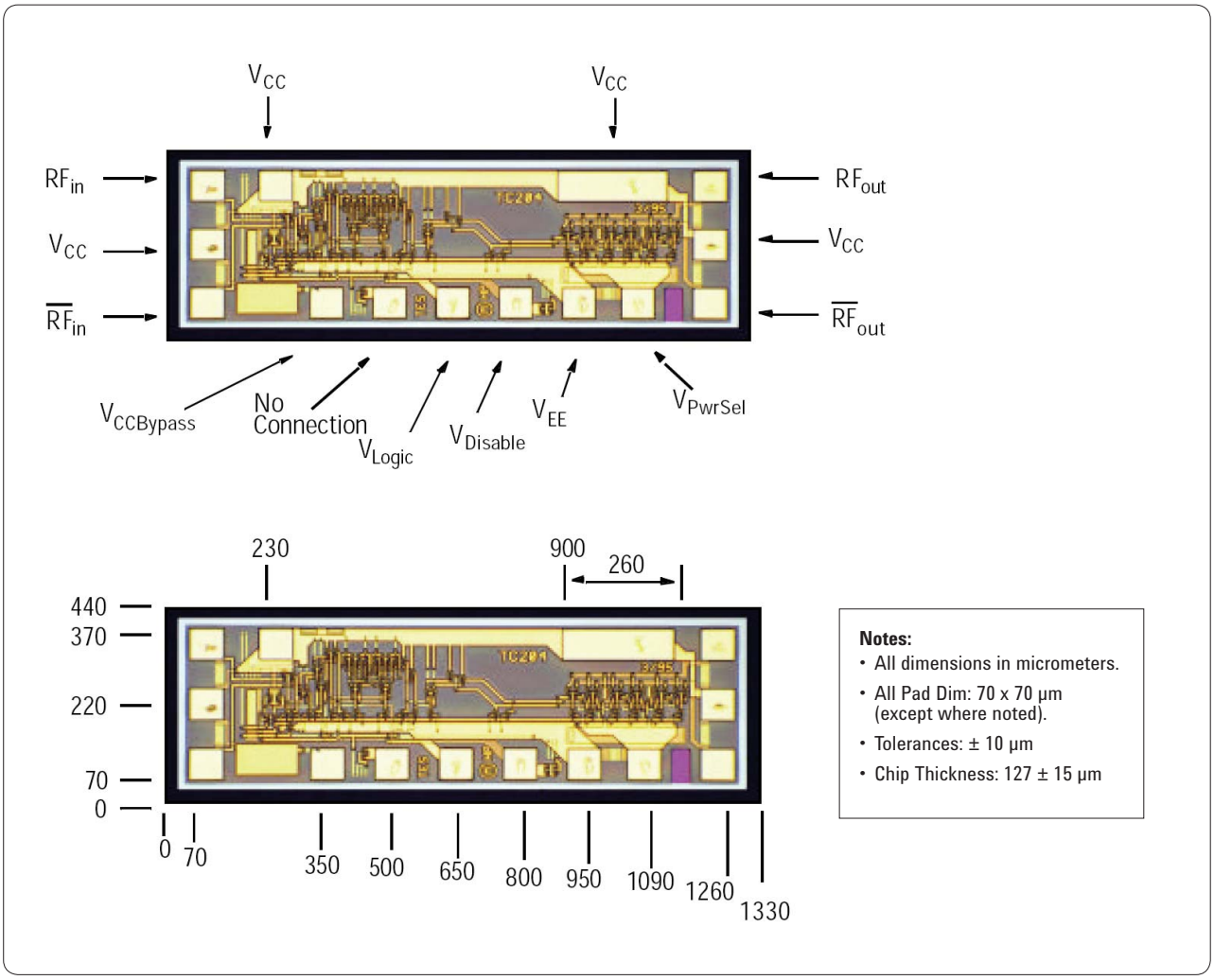


Figure 2. Pad locations and chip dimensions

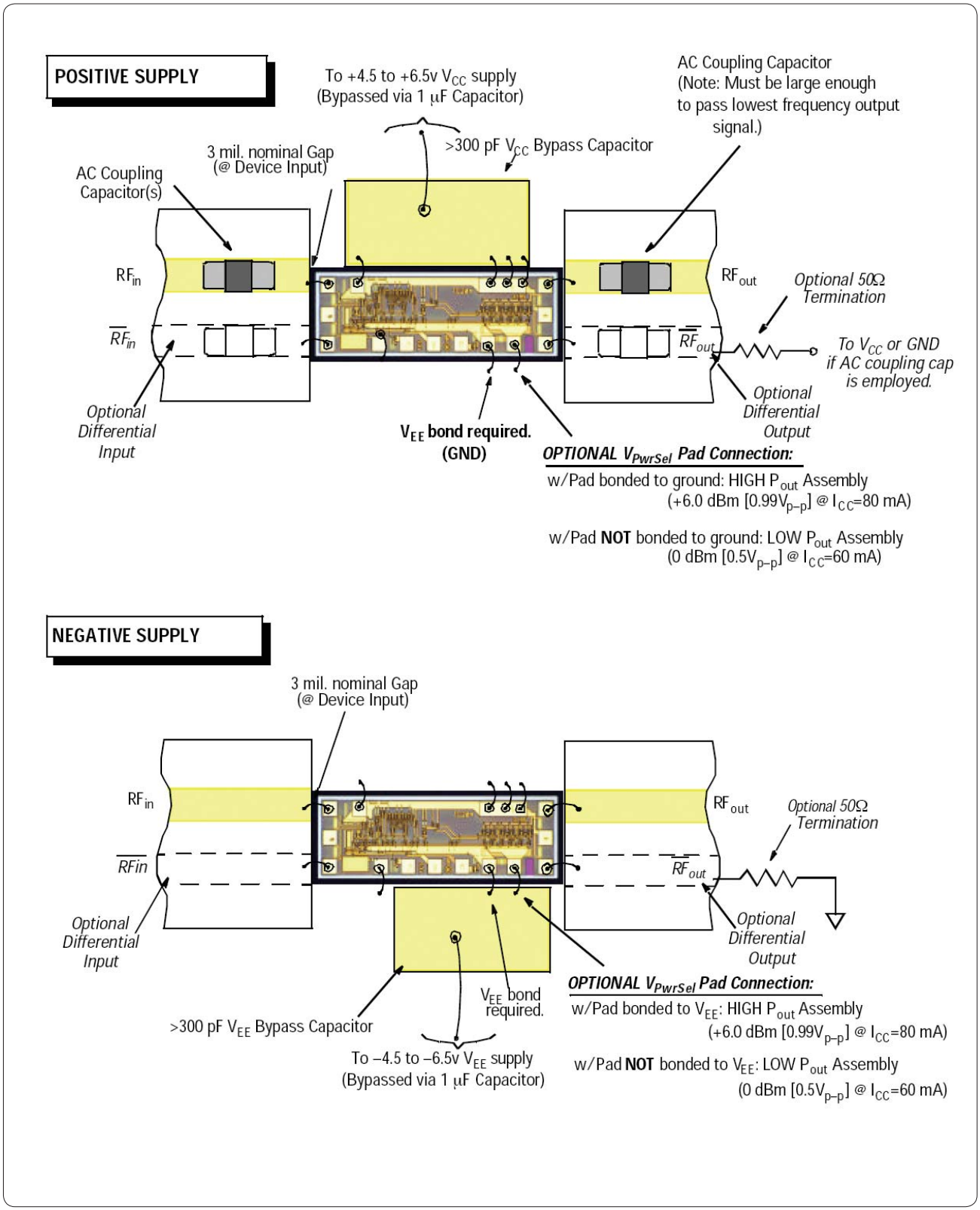


Figure 3. Assembly diagrams

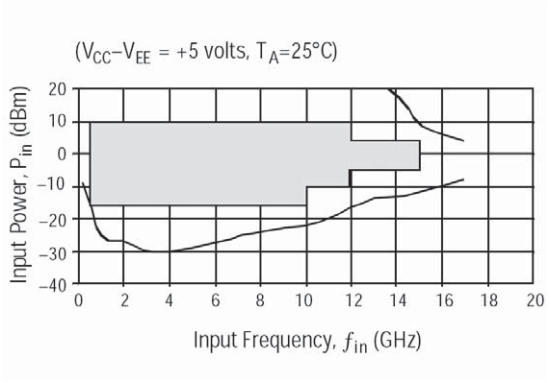


Figure 4. Typical input sensitivity window

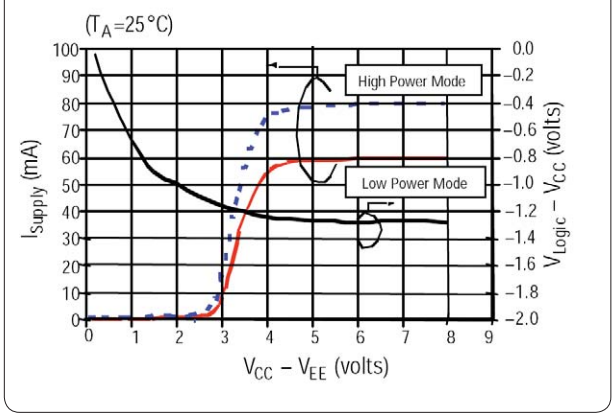


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

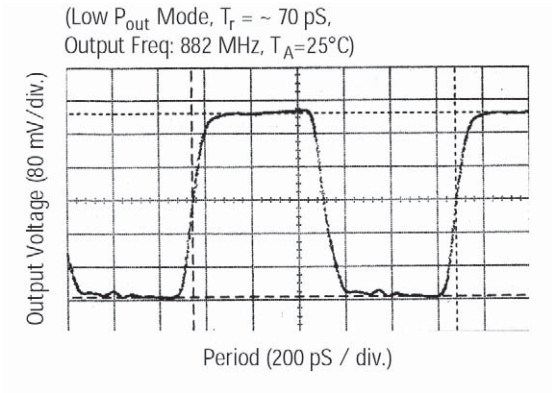


Figure 6. Typical output voltage waveform

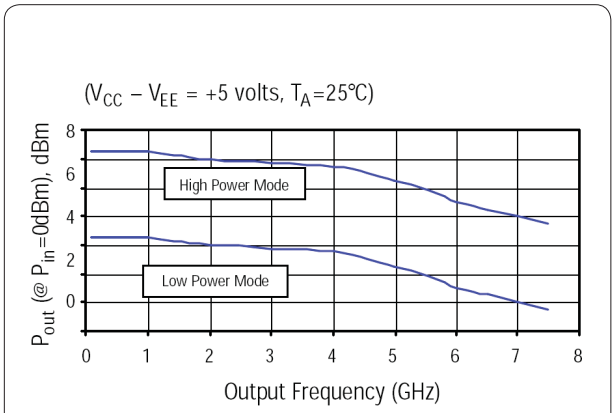


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

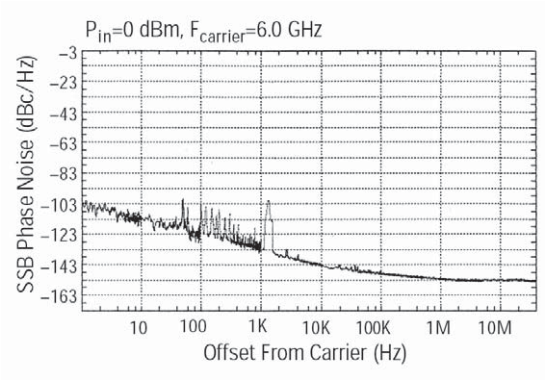


Figure 8. Typical phase noise performance

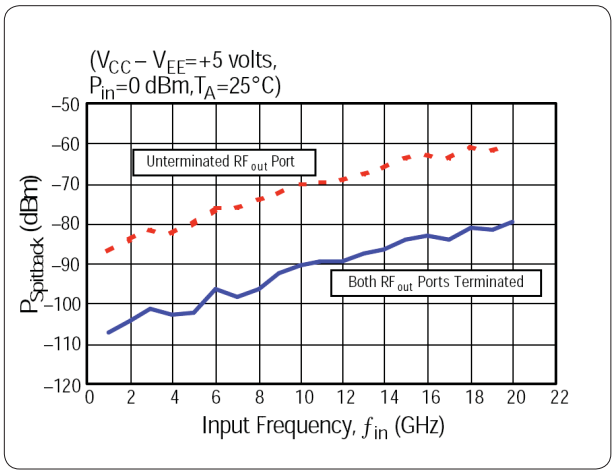


Figure 9. Typical "Spitback" power P(f_{out}) appearing at RF input port

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. Customers considering the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifications from Agilent.
In this data sheet the term typical refers to the 50th percentile performance.
For additional information contact Agilent

MMIC_Helpline@agilent.com.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus

Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

Printed in USA, November 20, 2007
5989-7343EN

Agilent Technologies

Agilent HMMC–3004
DC–16 GHz GaAs HBT MMIC
Divide–by–4 Prescaler

1GC1-8002

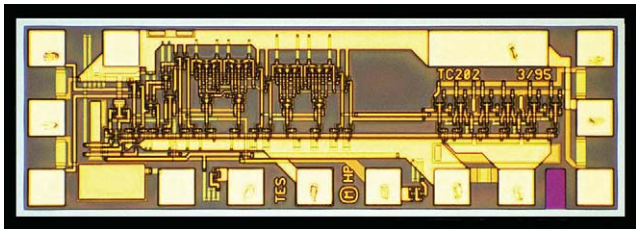
Data Sheet

Features

- **Wide Frequency Range: 0.2-16 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -20 to +10 dBm (1–10 GHz) -15 to +10 dBm (10–12 GHz) -10 to +5 dBm (12–15 GHz)**
- **Dual-mode P_{out}: (Chip Form) +6.0 dBm (0.99 Vp–p) @ 80 mA 0 dBm (0.5 Vp–p) @ 60 mA**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range: 4.5 to 6.5 volt operating range**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-3004 GaAs HBT MMIC Prescaler offers dc to 16 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise. In addition to the features listed above the device offers an input disable contact pad to eliminate any self-oscillation condition.



Chip Size: 1330 x 440 µm (52.4 x 17.3 mils)
Chip Size Tolerance: ± 10 µm (± 0.4 mils)
Chip Thickness: 127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions: 70 x 70 µm (2.8 x 2.8 mils)

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
$V_{Disable}$	Pre-amp disable voltage	V_{EE}	V_{CC}	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF Input Power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF_{in}}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ $T_{BS} \leq 85°C$. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

Agilent Technologies

dc Specifications/Physical Properties

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current (**HIGH** Output Power Configuration[2]: $V_{PwrSel} = V_{EE}$)	68	80	92	mA
	Bias supply current (**LOW** Output Power Configuration: V_{PwrSel} = open)	51	60	69	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.35	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.
2. High output power configuration: P_{out} = +6.0 dBm (V_{out} = 0.99 V_{p-p}). Low output power configuration: P_{out} = -0 dBm (V_{out} = 0.5 V_{p-p})

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	16	18		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self\text{-}Osc.}$	Output Self-Oscillation Frequency[2]		3.4		GHz
P_{in}	@ dc, (Square-wave input)	-15	≥ 25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	≥ 20	+10	dBm
	f_{in} = 1 to 10 GHz	-15	≥ 25	+10	dBm
	f_{in} = 10 to 12 GHz	-10	≥ 15	+10	dBm
	f_{in} = 12 to 15 GHz	-4	≥ 10	+4	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 12 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 12 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero–crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output edge speed (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave inpout signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Pre-amp Disable ($V_{Disable}$) feature, or the Differential Input de-biasing technique.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
		High Output Power Operating Mode[1]			
P_{out}	@ f_{out} < 1 GHz	4	6		dBM
	@ f_{out} = 2.5 GHz	4	6		dBm
	@ f_{out} = 3.5 GHz	3	5		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.79	0.99		volts
	@ f_{out} = 2.5 GHz	0.79	0.99		volts
	@ f_{out} = 3.5 GHz	0.7	0.88		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 12 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-48		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-68		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in})		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out} (f_{out}))		-25		dBc
		Low Output Power Operating Mode[2]			
P_{out}	@ f_{out} < 1 GHz	-2	0		dBm
	@ f_{out} = 2.5 GHz	-2	0		dBm
	@ f_{out} = 3.5 GHz	-3.0	-1.0		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.39	0.5		volts
	@ f_{out} = 2.5 GHz	0.39	0.5		volts
	@ f_{out} = 3.5 GHz	0.35	0.44		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 12 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-57		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-77		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in}))		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out} (f_{out}))		-30		dBc

Notes

1. $V_{PwrSel} = V_{EE}$.
2. V_{PwrSel} = Open Circuit.

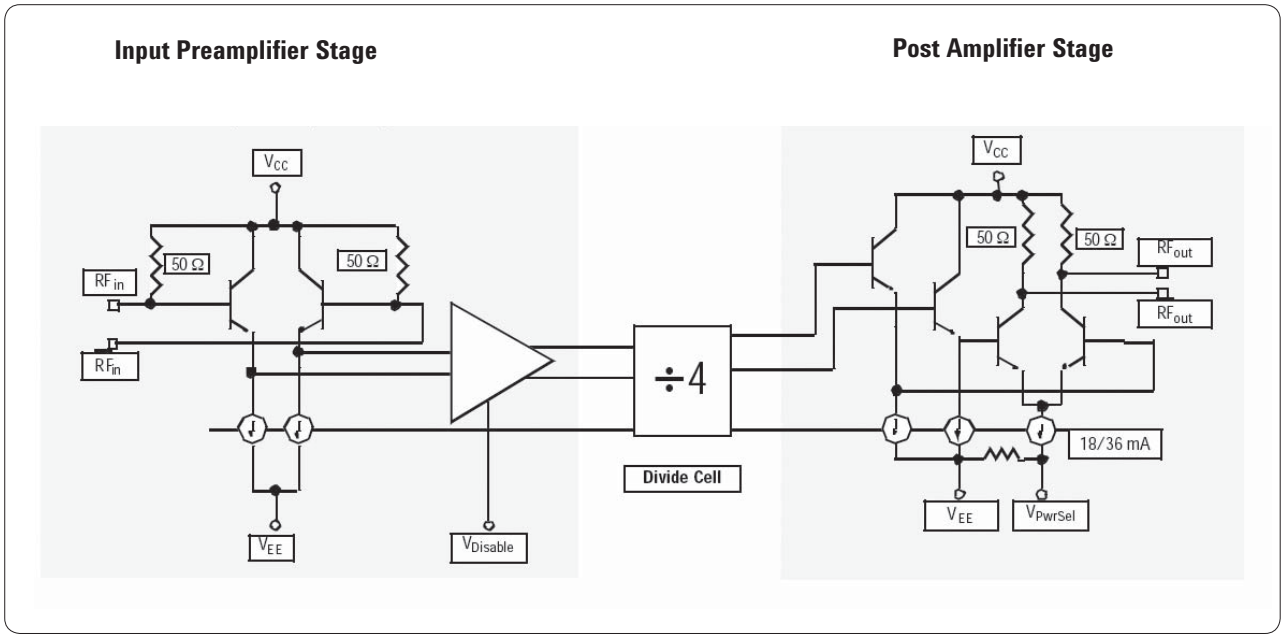


Figure 1. Simplified Schematic

Applications

The HMMC-3004 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 16 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

The device may be biased from either a single positive or single negative supply bias. The backside of the device is not dc connected to any dc bias point on the device.

For positive supply operation V_{CC} is nominally biased at any voltage in the +4.5 to +6.5 volt range with V_{EE} (or V_{EE} & V_{PwrSel}) grounded. For negative bias operation V_{CC} is typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to V_{EE} (or V_{EE} & V_{PwrSel}).

Several features are designed into this prescaler:

1. Dual-Output Power Feature
Bonding both V_{EE} and V_{PwrSel} pads to either ground (positive bias mode) or the negative supply (negative bias mode), will deliver ~0 dBm [0.5 V_{p-p}] at the RF output port while drawing ~40 mA supply current. Eliminating the V_{PwrSel} connection results in reduced output power and voltage swing, -6.0 dBm [0.25 V_{p-p}] but at a reduced current draw of ~30 mA resulting in less overall power dissipation.

(NOTE: V_{EE} must ALWAYS be bonded and V_{PwrSel} must NEVER be biased to any potential other than V_{EE} or open-circuited.)

2. V_{Logic} ECL Contact Pad
Under normal conditions no connection or external bias is required to this pad and it is self-biased to the on-chip ECL logic threshold voltage (V_{CC} -1.35 V). The user can provide an external bias to this pad (1.5 to 1.2 volts less than V_{CC}) to force the pre-scaler to operate at a system-generated logic threshold voltage.

3. Input Disable Feature
If an RF signal with sufficient signal-to-noise ratio is present at the RF input, the prescaler will operate and provide a divided output equal to the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the device may "self-oscillate", especially under small signal input powers or with only noise present at the input. This "self-oscillation" will produce an undesired output signal, also known as a false trigger. By applying an external bias to the input disable contact pad (more positive than V_{CC} -1.35 V), the input preamplifier stage is locked into either logic *"high"* or logic *"low"* preventing frequency division and any self-oscillation frequency which may be present.

4. Input dc Offset
Another method used to prevent false triggers or self-oscillation conditions is to apply a 20 to 100 mV dc offset voltage between the RF_{in} and $\overline{RF}_{in}$ ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 kΩ resistor between the used RF input to a contact point at the V_{EE} potential will result in an offset of ~25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

Assembly Techniques

Figure 3 shows the chip assembly diagram for single-ended I/O operation through 12 GHz for either positive or negative bias supply operation. In either case the supply contact to the chip must be capacitively bypassed to provide good input sensitivity and low input power feedthrough. Independent of the bias applied to the device, the backside of the chip should always be connected to both a good RF ground plane and a good thermal heat sinking region on the mounting surface.

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not dc grounded, the RF ports should be ac coupled via series capacitors mounted on the thin-film substrate at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the device backside may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

All bonds between the device and this bypass capacitor should be as short as possible to limit the inductance. For operation at frequencies below 1 GHz, a large value capacitor must be added to provide proper RF bypassing.

Due to on-chip 50 Ω matching resistors at all four RF ports, no external termination is required on any unused RF port. However, improved *"Spitback"* performance (~20 dB) and input sensitivity can be achieved by terminating the unused RF_{out} port to V_{CC} through 50 Ω (positive supply) or to ground via a 50 Ω termination (negative supply operation).

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Optional dc Operating Values/Logic Levels

(T_A = 25°C)

Function	Symbol	Conditions	Min (volts/mA)	Typical (volts/mA)	Max (volts/mA)
Logic Threshold[1]	V_{Logic}		V_{CC}-1.5	V_{CC}-1.35	V_{CC}-1.2
Input Disable	$V_{Disable(High)}$ [Disable]		V_{Logic} + 0.25	V_{Logic}	V_{CC}
Input Disable	$V_{Disable(Low)}$ [Enable]		V_{EE}	V_{Logic}	V_{Logic} - 0.25
Input Disable	$I_{Disable}$	$V_D > V_{EE}+3$	($V_{Disable}$ -V_{EE} -3)/500	($V_{Disable}$ -V_{EE} -3)/500	($V_{Disable}$ -V_{EE} -3)/500
Input Disable	$I_{Disable}$	$V_D < V_{EE}+3$	0	0	0

Note:
1. Acceptable voltage range when applied from external source.

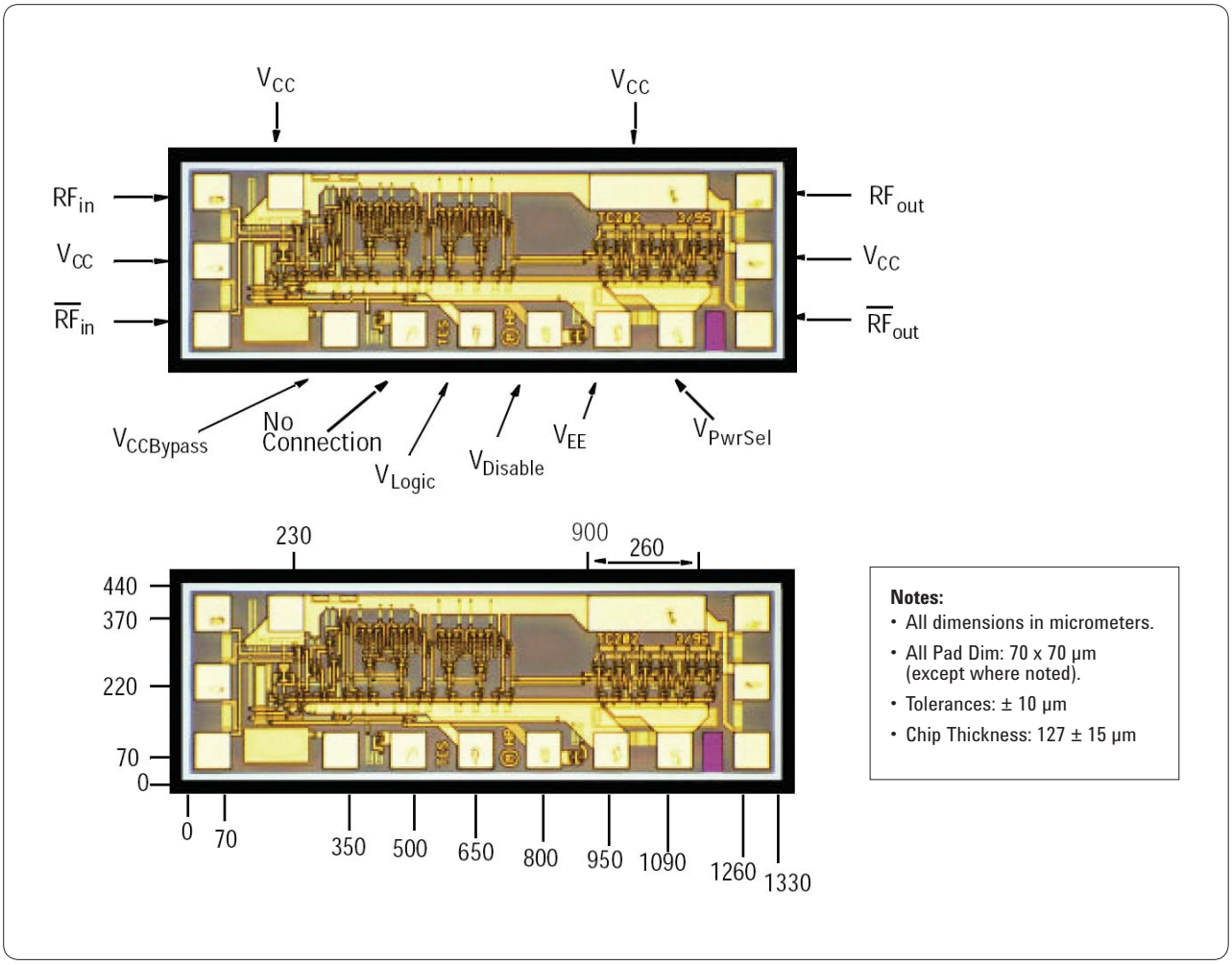


Figure 2. Pad locations and chip dimensions

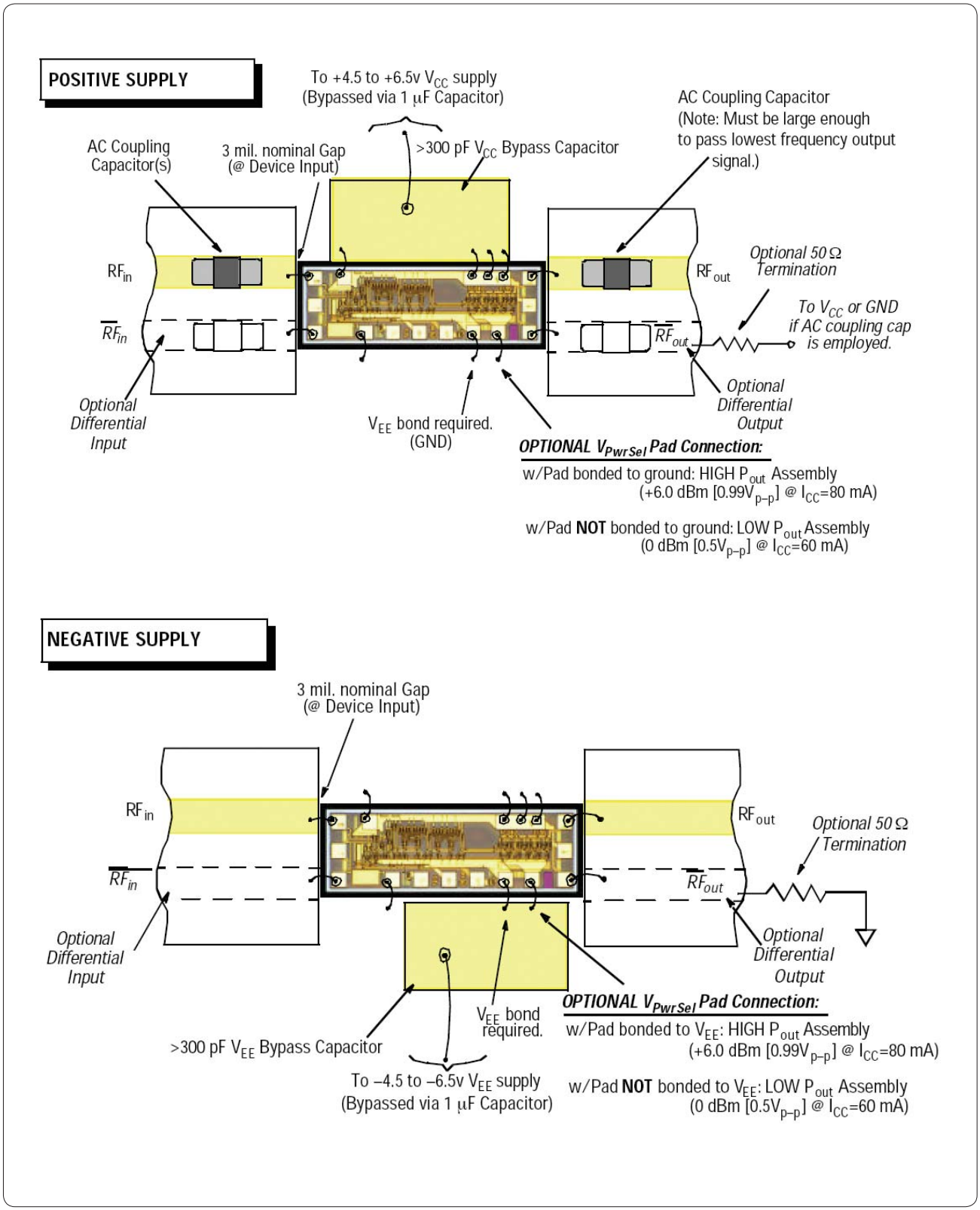


Figure 3. Assembly diagrams

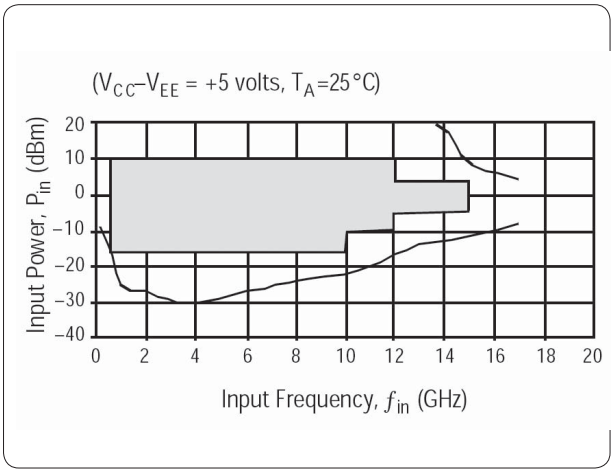


Figure 4. Typical input sensitivity window

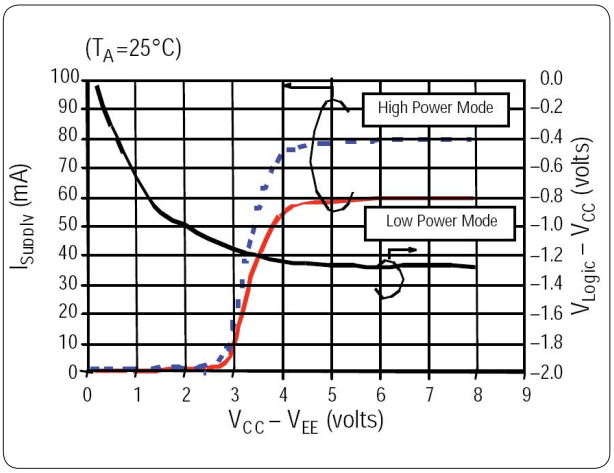


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

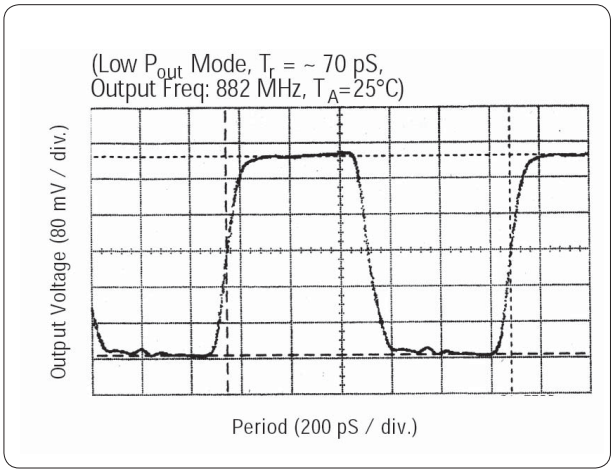


Figure 6. Typical output voltage waveform

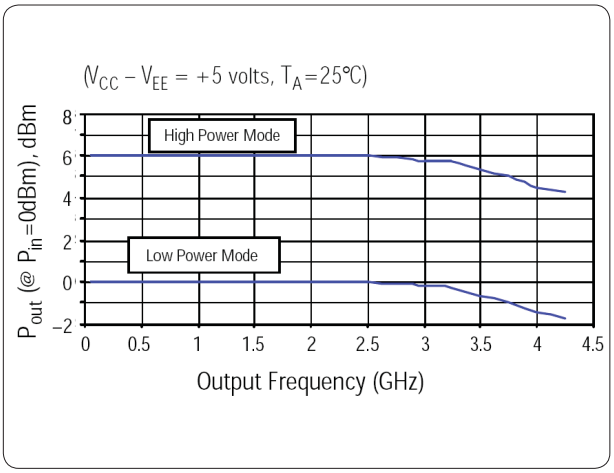


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

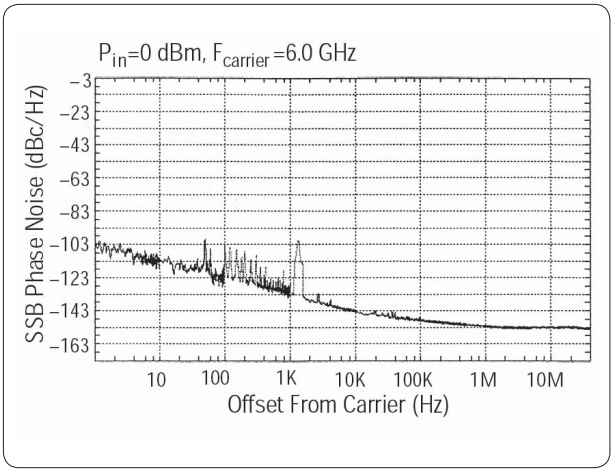


Figure 8. Typical phase noise performance

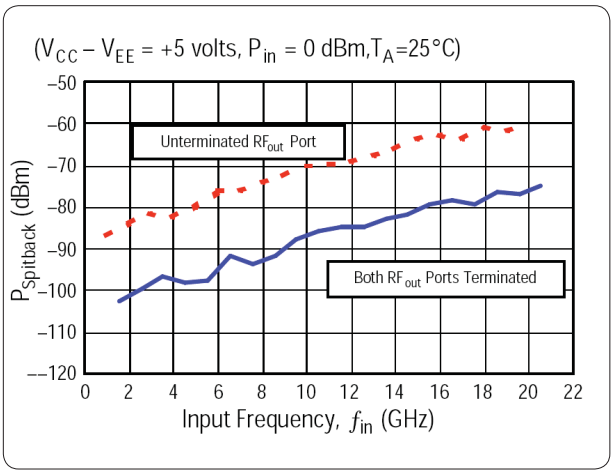


Figure 9. Typical "Spitback" power P(f_{out}) appearing at RF input port

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. Customers considering the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifications from Agilent.
In this data sheet the term typical refers to the 50th percentile performance.
For additional information contact Agilent

MMIC_Helpline@agilent.com.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus
Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

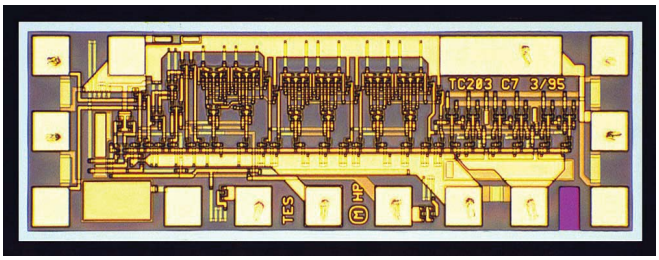
Printed in USA, November 19, 2007
5989-7344EN

Agilent Technologies

Agilent HMMC–3008
DC–16 GHz GaAs HBT MMIC
Divide–by–8 Prescaler

1GC1-8003

Data Sheet



Chip Size: 1330 x 440 µm (52.4 x 17.3 mils)
Chip Size Tolerance: ± 10 µm (± 0.4 mils)
Chip Thickness: 127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions: 70 x 70 µm (2.8 x 2.8 mils)

Features

- **Wide Frequency Range: 0.2–16 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -20 to +10 dBm (1–10 GHz) -15 to +10 dBm (10–12 GHz) -10 to +5 dBm (12–15 GHz)**
- **Dual-mode P_{out}: (Chip Form) +6.0 dBm (0.99 V_{p-p}) @ 80 mA 0 dBm (0.5 V_{p-p}) @ 60 mA**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range: 4.5 to 6.5 volt operating range**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-3008 GaAs HBT MMIC prescaler offers dc to 16 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler pro-vides a large input power sensitivity window and low phase noise. In addition to the features listed above the device offers an input disable contact pad to eliminate any self-oscillation condition.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
$V_{Disable}$	Pre-amp disable voltage	V_{EE}	V_{CC}	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -0.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF_{in}}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ T_{BS} ≤85 °C. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

Agilent Technologies

dc Specifications/Physical Properties

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current (**HIGH** Output Power Configuration[2]: $V_{PwrSel} = V_{EE}$)	73	86	99	mA
	Bias supply current (**LOW** Output Power Configuration: V_{PwrSel} = open)	56	66	76	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.35	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified suply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.
2. High output power configuration: P_{out} = +6.0 dBm (V_{out} = 0.99 V_{p-p}). Low output power configuration: P_{out} = 0 dBm (V_{out} = 0.5 V_{p-p})

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	16	18		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self-Osc.}$	Output Self-Oscillation Frequency[2]		1.7		GHz
P_{in}	@ dc, (Square-wave input)	-15	> -25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	> 20	+10	dBm
	f_{in} = 1 to 10 GHz	-15	> -25	+10	dBm
	f_{in} = 10 to 12 GHz	-10	> -15	+10	dBm
	f_{in} = 12 to 15 GHz	-4	> -10	+4	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 12 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 12 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero-crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output edge speed (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave input signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Pre-amp Disable ($V_{Disable}$) feature, or the Differential Input de-biasing technique.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
		High Output Power Operating Mode[1]			
P_{out}	@ f_{out} < 1 GHz	4.0	6.0		dBM
	@ f_{out} = 1.25 GHz	4.0	6.0		dBm
	@ f_{out} = 1.5 GHz	3.7	5.7		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} <1 GHz	0.79	0.99		volts
	@ f_{out} = 1.25 GHz	0.79	0.99		volts
	@ f_{out} = 1.5 GHz	0.76	0.96		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 12 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-55		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-75		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to $P_{in}(f_{in})$		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 1.5 GHz, referred to P_{out} (f_{out}))		-30		dBc
		Low Output Power Operating Mode[2]			
P_{out}	@ f_{out} < 1 GHz	-2	0		dBm
	@ f_{out} = 1.25 GHz	-2	0		dBm
	@ f_{out} = 1.5 GHz	-2.3	-0.3		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.39	0.5		volts
	@ f_{out} = 1.25 GHz	0.39	0.5		volts
	@ f_{out} = 1.5 GHz	0.38	0.48		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 12 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-65		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-85		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in}))		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 1.5 GHz, referred to P_{out} (f_{out}))		-35		dBc

Notes

1. $V_{PwrSel} = V_{EE}$.
2. V_{PwrSel} = Open Circuit.

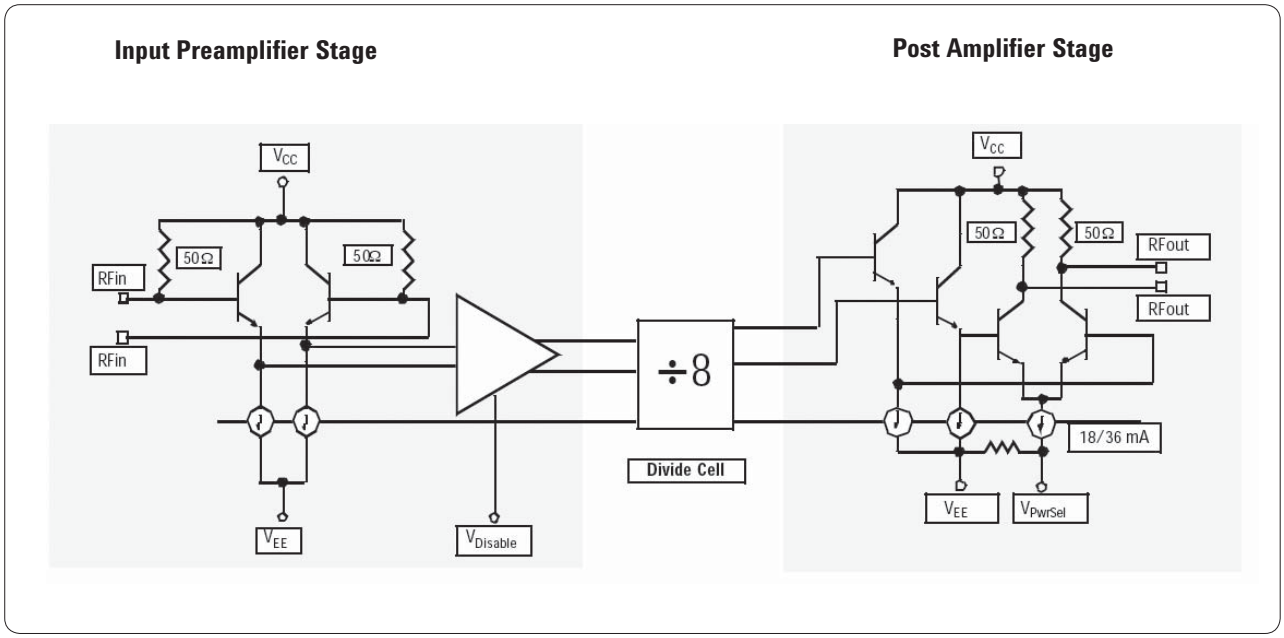


Figure 1. Simplified Schematic

Applications

The HMMC-3008 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 16 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

The device may be biased from either a single positive or single negative supply bias. The back-side of the device is not dc connected to any dc bias point on the device.

For positive supply operation V_{CC} is nominally biased at any voltage in the +4.5 to +6.5 volt range with V_{EE} (or V_{EE} & V_{PwrSel}) grounded. For negative bias operation V_{CC} is typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to V_{EE} (or V_{EE} & V_{PwrSel}).

Several features are designed into this prescaler:

1. Dual-Output Power Feature
Bonding both V_{EE} and V_{PwrSel} pads to either ground (positive bias mode) or the negative supply (negative bias mode), will deliver ~0 dBm [0.5 V_{p-p}] at the RF output port while drawing ~40 mA supply current. Eliminating the V_{PwrSel} connection results in reduced output power and voltage swing, -6.0 dBm [0.25 V_{p-p}] but at a reduced current draw of ~30 mA resulting in less overall power dissipation. (NOTE: V_{EE} must ALWAYS be bonded and V_{PwrSel} must NEVER be biased to any potential other than V_{EE} or open-circuited.)

2. V_{Logic} ECL Contact Pad
Under normal conditions no connection or external bias is required to this pad and it is self-biased to the on-chip ECL logic threshold voltage (V_{CC} -1.35 V). The user can provide an external bias to this pad (1.5 to 1.2 volts less than V_{CC}) to force the prescaler to operate at a system generated logicthreshold voltage.

3. Input Disable Feature
If an RF signal with sufficient signal-to-noise ratio is present at the RF input, the prescaler will operate and provide a divided output equal to the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the device may "self-oscillate", especially under small signal input powers or with only noise present at the input This "self-oscillation" will produce a undesired output signal also known as a false trigger. By applying an external bias to the input disable contact pad (more positive than V_{CC} -1.35 V), the input preamplifier stage is locked into either logic "high" or logic "low" preventing frequency division and any self-oscillation frequency which may be present.

4. Input dc Offset
Another method used to prevent false triggers or self-oscillation conditions is to apply a 20 to 100 mV dc offset voltage between the RF_{in} and RF_{in} ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 kW resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ≈25 mV between the $\overline{RF}$ inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

Assembly Techniques

Figure 3 shows the chip assembly diagram for single-ended I/O operation through 12 GHz for either positive or negative bias supply operation. In either case the supply contact to the chip must be capacitively bypassed to provide good input sensitivity and low input power feedthrough. Independent of the bias applied to the device, the backside of the chip should always be connected to both a good RF ground plane and a good thermal heat sinking region on the mounting surface.

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not dc grounded, the RF ports should be ac coupled via series capacitors mounted on the thin-film substrate at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the device backside may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

All bonds between the device and this bypass capacitor should be as short as possible to limit the inductance. For operation at frequencies below 1 GHz, a large value capacitor must be added to provide proper RF bypassing.

Due to on-chip 50 Ω matching resistors at all four RF ports, no external termination is required on any unused RF port. However, improved *"Spitback"* performance (~20 dB) and input sensitivity can be achieved by terminating the unused RFout port to V_{CC} through 50 Ω (positive supply) or to ground via a 50 Ω termination (negative supply operation).

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Optional dc Operating Values/Logic Levels

(T_A = 25°C)

Function	Symbol	Conditions	Min (volts/mA)	Typical (volts/mA)	Max (volts/mA)
Logic Threshold[1]	V_{Logic}		V_{CC}-1.5	V_{CC}-1.35	V_{CC}-1.2
Input Disable	$V_{Disable(High)}$ [Disable]		V_{Logic}+0.25	V_{Logic}	V_{CC}
Input Disable	$V_{Disable(Low)}$ [Enable]		V_{EE}	V_{Logic}	V_{Logic}-0.25
Input Disable	$I_{Disable}$	$V_D > V_{EE}$+3	($V_{Disable}$-V_{EE} -3)/500	($V_{Disable}$-V_{EE} -3)/500	($V_{Disable}$-V_{EE} -3)/500
Input Disable	$I_{Disable}$	$V_D < V_{EE}$+3	0	0	0

Note:
1. Acceptable voltage range when applied from external source.

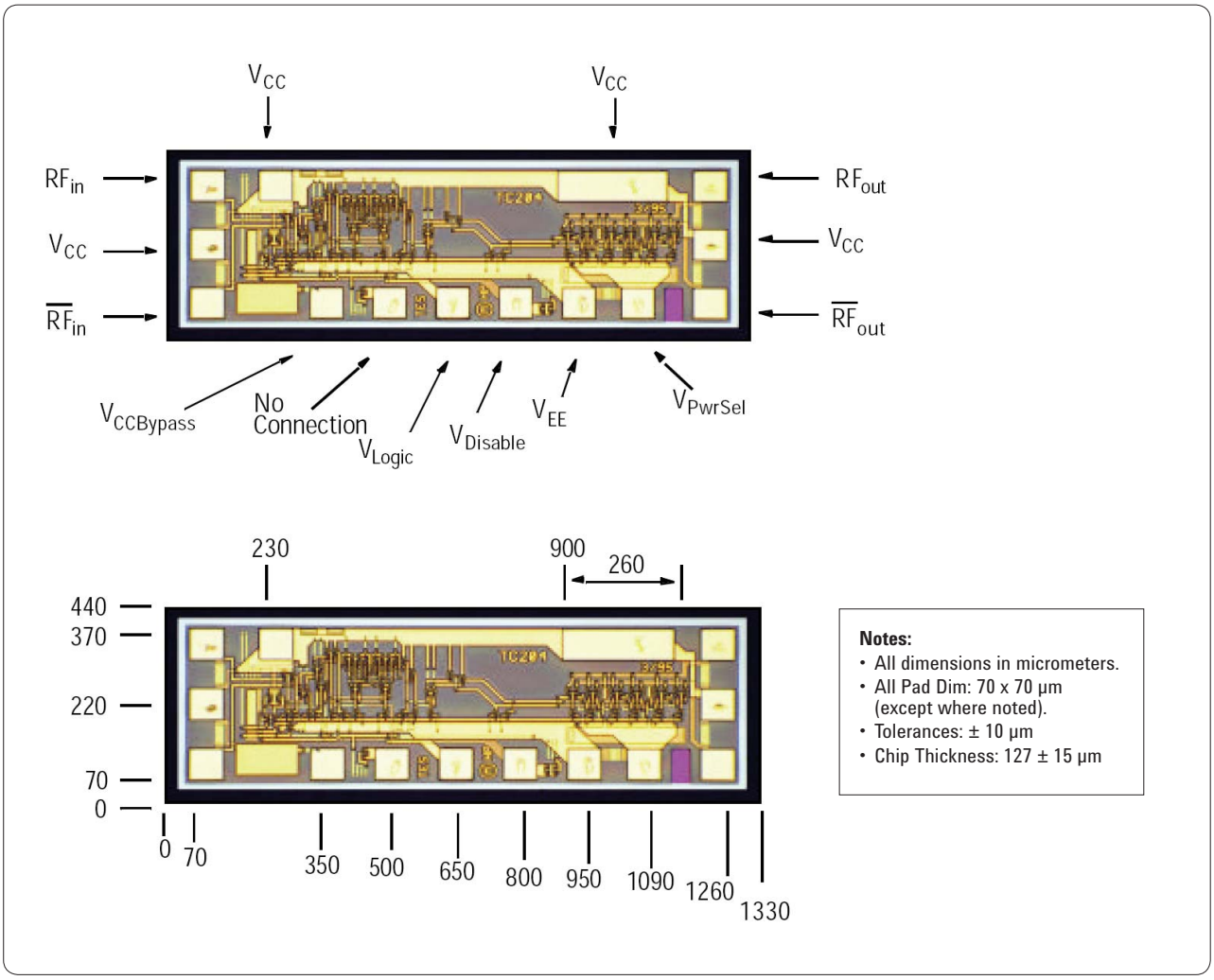


Figure 2. Pad locations and chip dimensions

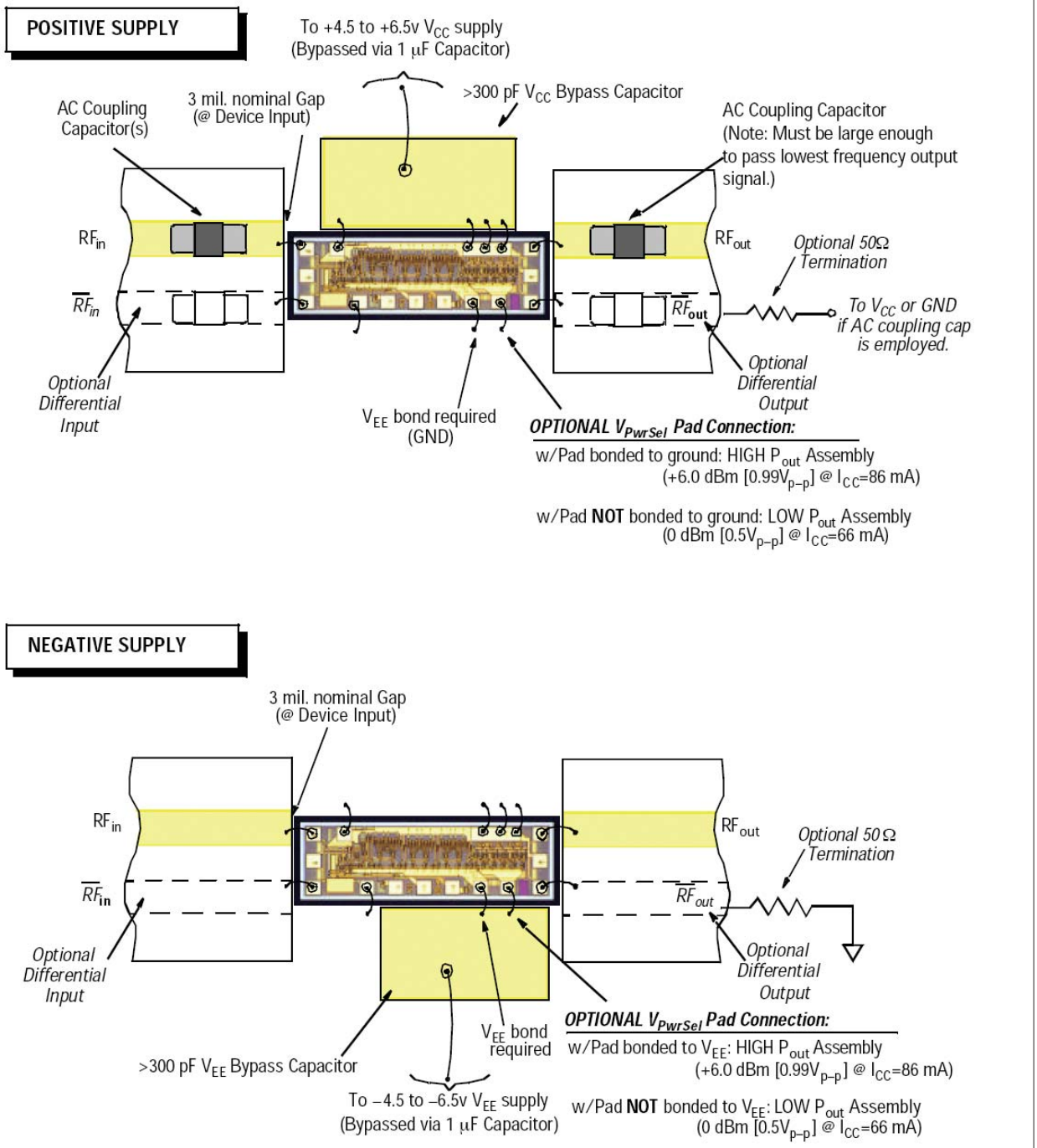


Figure 3. Assembly diagrams

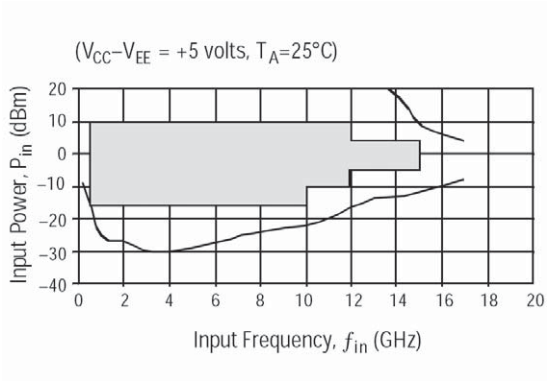


Figure 4. Typical input sensitivity window

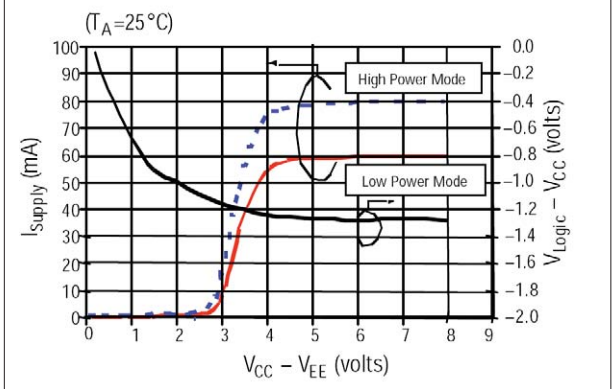


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

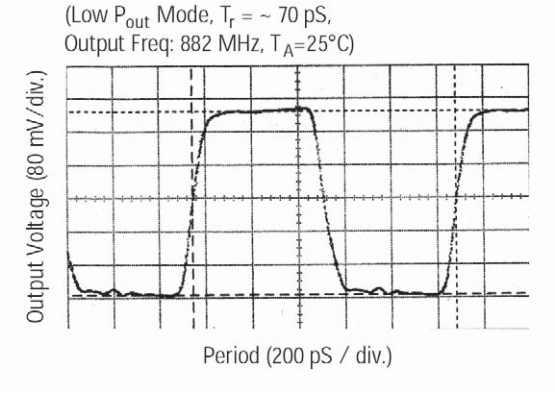


Figure 6. Typical output voltage waveform

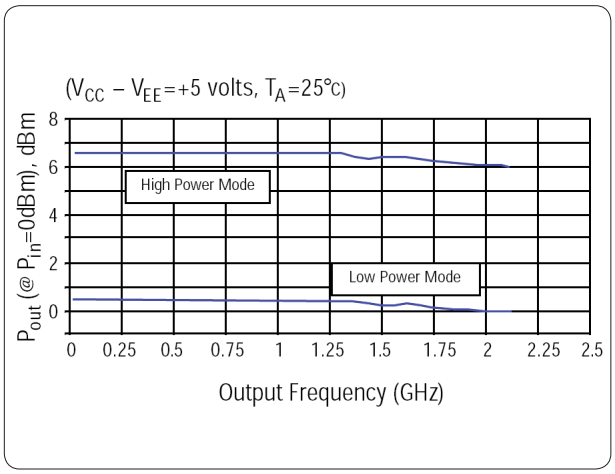


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

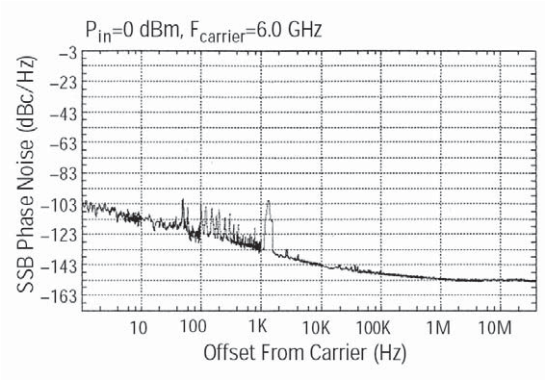


Figure 8. Typical phase noise performance

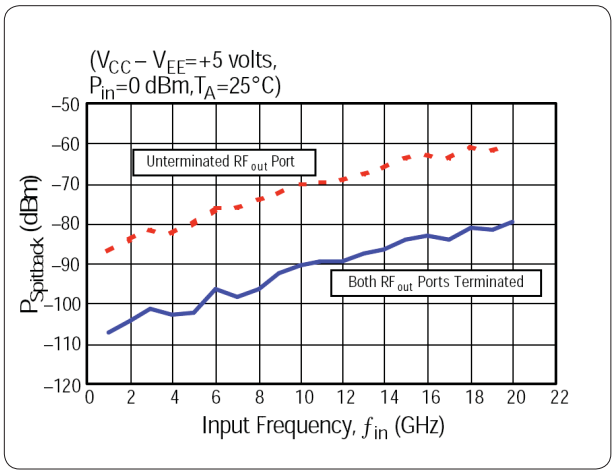


Figure 9. Typical "Spitback" power P(f_{out}) appearing at RF input port

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

LXI

www.lxistandard.org
LXI is the LAN-based successor to GPIB, providing faster, more efficient connectivity. Agilent is a founding member of the LXI consortium.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete listof circuit specifications. Customers consider-ing the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifi cations from Agilent. In this data sheet the term typical refers to the 50th percentile performance. For additional information contact Agilent

MMIC_Helpline@agilent.com.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus
Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

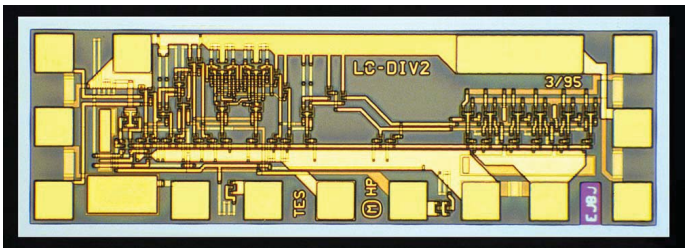
Printed in USA, November 20, 2007
5989-7345EN

Agilent Technologies

Agilent HMMC–3022
DC–12 GHz High Efficiency GaAs HBT MMIC Divide–by–2 Prescaler

1GC1-8009

Data Sheet



Chip Size: 1330 x 440 µm (52.4 x 17.3 mils)
Chip Size Tolerance: ± 10 µm (± 0.4 mils)
Chip Thickness: 127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions: 70 x 70 µm (2.8 x 2.8 mils)

Features

- **Wide Frequency Range: 0.2-12 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -20 to +10 dBm (1–8 GHz) -15 to +10 dBm (8–10 GHz) -10 to +4 dBm (10–12 GHz)**
- **Dual-mode P_{out}: (Chip Form) 0 dBm (0.5 V_{p-p}) @ 40 mA -6.0 dBm (0.25 V_{p-p}) @ 30 mA**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range: 4.5 to 6.5 volt operating range**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-3022 GaAs HBT MMIC prescaler offers dc to 12 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise. In addition to the features listed above the device offers an input disable contact pad to eliminate any self-oscillation condition.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
$V_{Disable}$	Pre-amp disable voltage	V_{EE}	V_{CC}	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ $T_{BS} \leq 85°C$. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

dc Specifications/Physical Properties

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current (**HIGH** Output Power Configuration[2]: $V_{PwrSel} = V_{EE}$)	34	40	46	mA
	Bias supply current (**LOW** Output Power Configuration: V_{PwrSel} = open)	25	30	35	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.35	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.
2. High output power configuration: P_{out} = 0 dBm (V_{out} = 0.5 V_{p-p}). Low output power configuration: P_{out} = -6.0 dBm (V_{out} = 0.25 V_{p-p})

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	12	14		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.3	GHz
$f_{Self-Osc.}$	Output Self-Oscillation Frequency[2]		6.8		GHz
P_{in}	@ dc, (Square-wave input)	-15	> -25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	> -20	+10	dBm
	f_{in} = 1 to 8 GHz	-15	> -20	+10	dBm
	f_{in} = 8 to 10 GHz	-10	> -15	+ 5	dBm
	f_{in} = 10 to 12 GHz	-5	> -10	-1	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 10 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 10 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero–crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output edge speed (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave inpout signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Pre-amp Disable ($V_{Disable}$) feature, or the Differential Input de-biasing technique.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	High Output Power Operating Mode[1] Min.	Typ.	Max.	Units
P_{out}	@ f_{out} < 1 GHz	-2	0		dBM
	@ f_{out} = 2.5 GHz	-2.5	-0.5		dBm
	@ f_{out} = 5.0 GHz	-4.5	-2.5		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.39	0.5		volts
	@ f_{out} = 2.5 GHz	0.37	0.47		volts
	@ f_{out} = 5.0 GHz	0.30	0.37		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 10 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-54		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-74		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 10 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in})		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 2.0 GHz, referred to P_{out} (f_{out}))		-25		dBc
		Low Output Power Operating Mode[2]			
P_{out}	@ f_{out} < 1 GHz	-8	-6		dBm
	@ f_{out} = 2.5 GHz	-8	-6		dBm
	@ f_{out} = 5.0 GHz	-10	-8		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.20	0.25		volts
	@ f_{out} = 2.5 GHz	0.20	0.25		volts
	@ f_{out} = 5.0 GHz	0.16	0.20		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 10 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-63		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-83		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 10 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in}))		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 2.0 GHz, referred to P_{out} (f_{out}))		-30		dBc

Notes

1. $V_{PwrSel} = V_{EE}$.
2. V_{PwrSel} = Open Circuit.

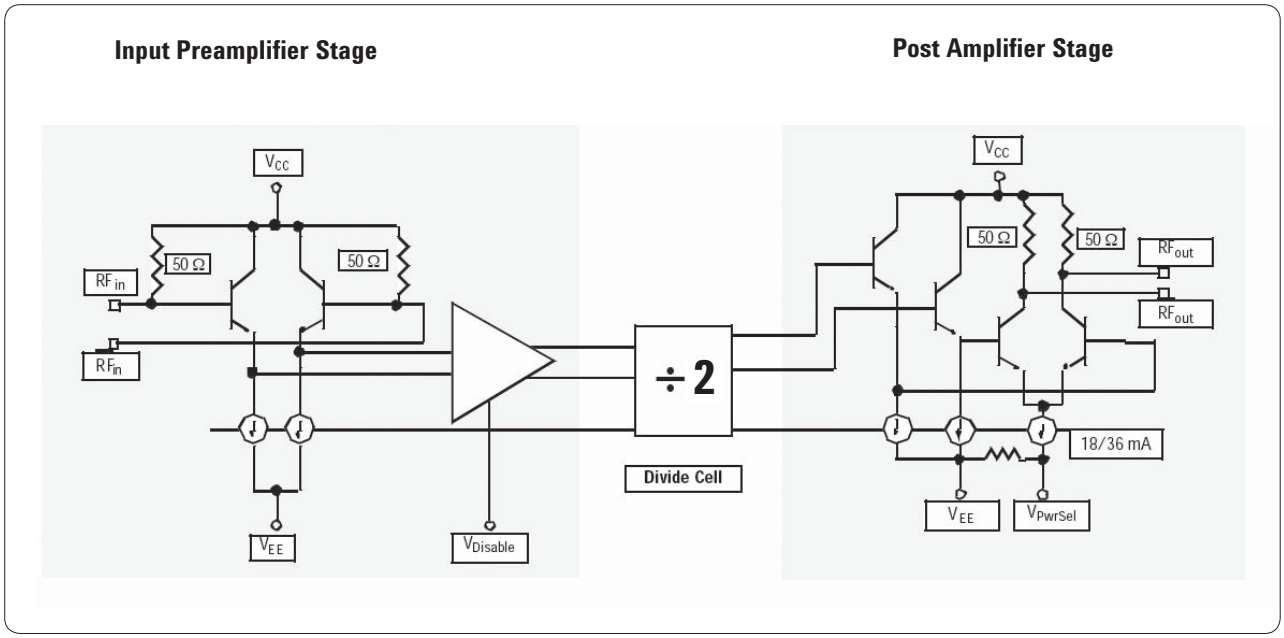


Figure 1. Simplified Schematic

Applications

The HMMC-3022is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 12 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

The device may be biased from either a single positive or single negative supply bias. The backside of the device is not dc connected to any dc bias point on the device.

For positive supply operation V_{CC} is nominally biased at any voltage in the +4.5 to +6.5 volt range with V_{EE} (or V_{EE} & V_{PwrSel}) grounded. For negative bias operation V_{CC} is typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to V_{EE} (or V_{EE} & V_{PwrSel}).

Several features are designed into this prescaler:

1. Dual-Output Power Feature
Bonding both V_{EE} and V_{PwrSel} pads to either ground (positive bias mode) or the negative supply (negative bias mode), will deliver ~0 dBm [0.5 V_{p-p}] at the RF output port while drawing ~40 mA supply current. Eliminating the V_{PwrSel} connection results in reduced output power and voltage swing, -6.0 dBm
[0.25 V_{p-p}] but at a reduced current draw of ~30 mA resulting in less overall power dissipation.

(NOTE: V_{EE} must ALWAYS be bonded and V_{PwrSel} must NEVER be biased to any potential other than V_{EE} or open–circuited.)

2. V_{Logic} ECL Contact Pad
Under normal conditions no connection or external bias is required to this pad and it is self-biased to the on-chip ECL logic threshold voltage (V_{CC} -1.35 V). The user can provide an external bias to this pad (1.5 to 1.2 volts less than V_{CC}) to force the prescaler to operate at a system generated logic threshold voltage.

3. Input Disable Feature
If an RF signal with sufficient signal-to-noise ratio is present at the RF input, the prescaler will operate and provide a divided output equal to the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the device may "self-oscillate," especially under small signal input powers or with only noise present at the input. This "self-oscillation" will produce a undesired output signal also known as a false trigger. By applying an external bias to the input disable contact pad (more positive than V_{CC} - 1.35 V), the input preamplifier stage is locked into either logic *"high"* or logic *"low"* preventing frequency division and any self-oscillation frequency which may be present.

4. Input dc Offset
Another method used to prevent false triggers or self-oscillation conditions is to apply a 20 to 100 mV dc offset voltage between the RF_{in} and $\overline{RF}_{in}$ ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 KΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ~25mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

Assembly Techniques

Figure 3 shows the chip assembly diagram for single-ended I/O operation through 12 GHz for either positive or negative bias supply operation. In either case the supply contact to the chip must be capacitively bypassed to provide good input sensitivity and low input power feedthrough. Independent of the bias applied to the device, the backside of the chip should always be connected to both a good RF ground plane and a good thermal heat sinking region on the mounting surface.

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 W resistors. Under any bias conditions where V_{CC} is not dc grounded, the RF ports should be ac coupled via series capacitors mounted on the thin-film substrate at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the device backside may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

All bonds between the device and this bypass capacitor should be as short as possible to limit the inductance. For operation at frequencies below 1 GHz, a large value capacitor must be added to provide proper RF bypassing.

Due to on-chip 50 Ω matching resistors at all four RF ports, no external termination is required on any unused RF port. However, improved *"Spitback"* performance (~20 dB) and input sensitivity can be achieved by terminating the unused RF_{out} port to V_{CC} through 50 Ω (positive supply) or to ground via a 50 Ω termination (negative supply operation).

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Optional dc Operating Values/Logic Levels

(T_A = 25°C)

Function	Symbol	Conditions	Min (volts/mA)	Typical (volts/mA)	Max (volts/mA)
Logic Threshold[1]	V_{Logic}		V_{CC}-1.5	V_{CC}-1.35	V_{CC}-1.2
Input Disable	$V_{Disable(High)}$ [Disable]		V_{Logic}+0.25	V_{Logic}	V_{CC}
Input Disable	$V_{Disable(Low)}$ [Enable]		V_{EE}	V_{Logic}	V_{Logic}-0.25
Input Disable	$I_{Disable}$	$V_D > V_{EE}$+3	($V_{Disable}$-V_{EE} -3)/500	($V_{Disable}$-V_{EE} -3)/500	($V_{Disable}$-V_{EE} -3)/500
Input Disable	$I_{Disable}$	$V_D < V_{EE}$+3	0	0	0

Note:
1. Acceptable voltage range when applied from external source.

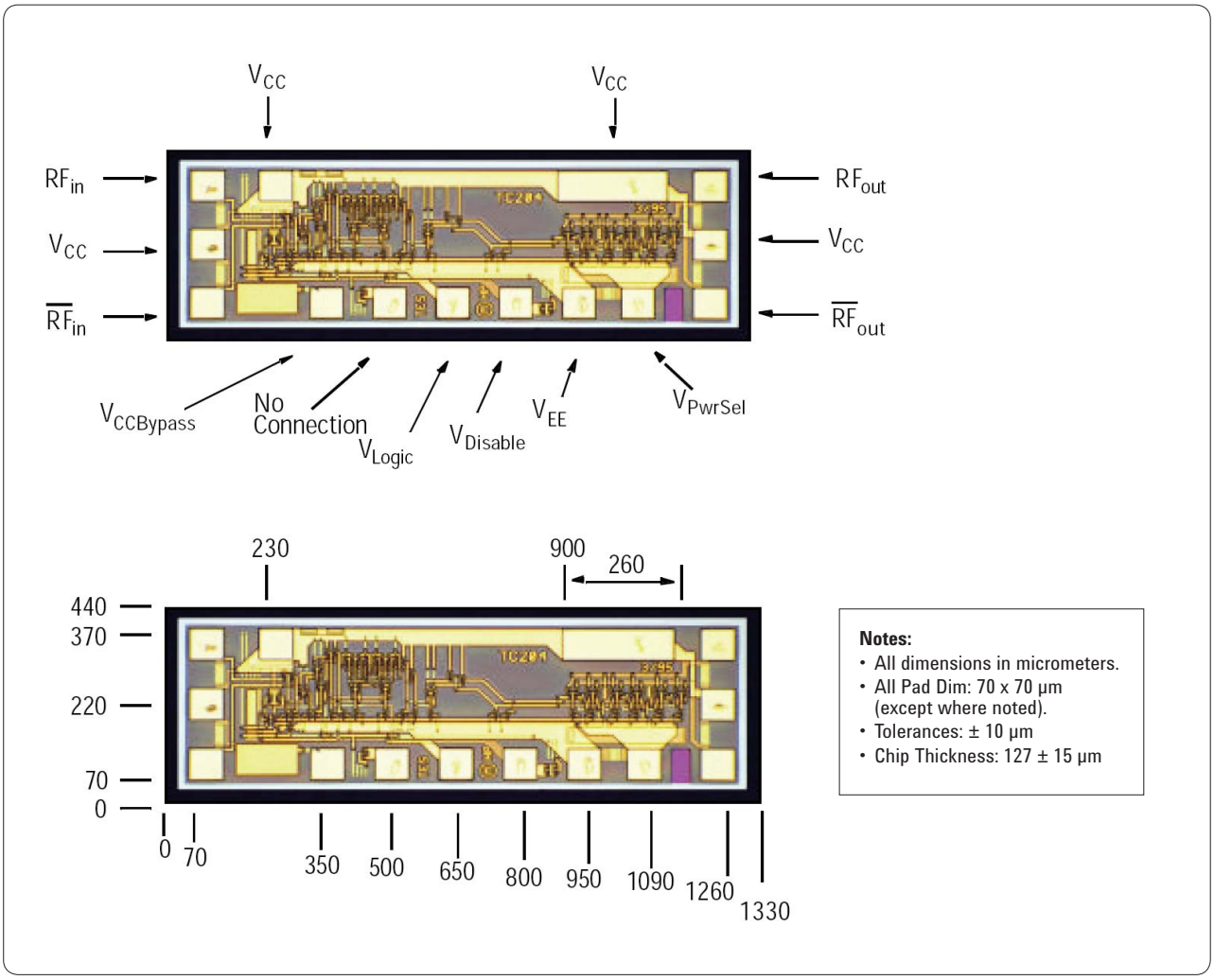


Figure 2. Pad locations and chip dimensions

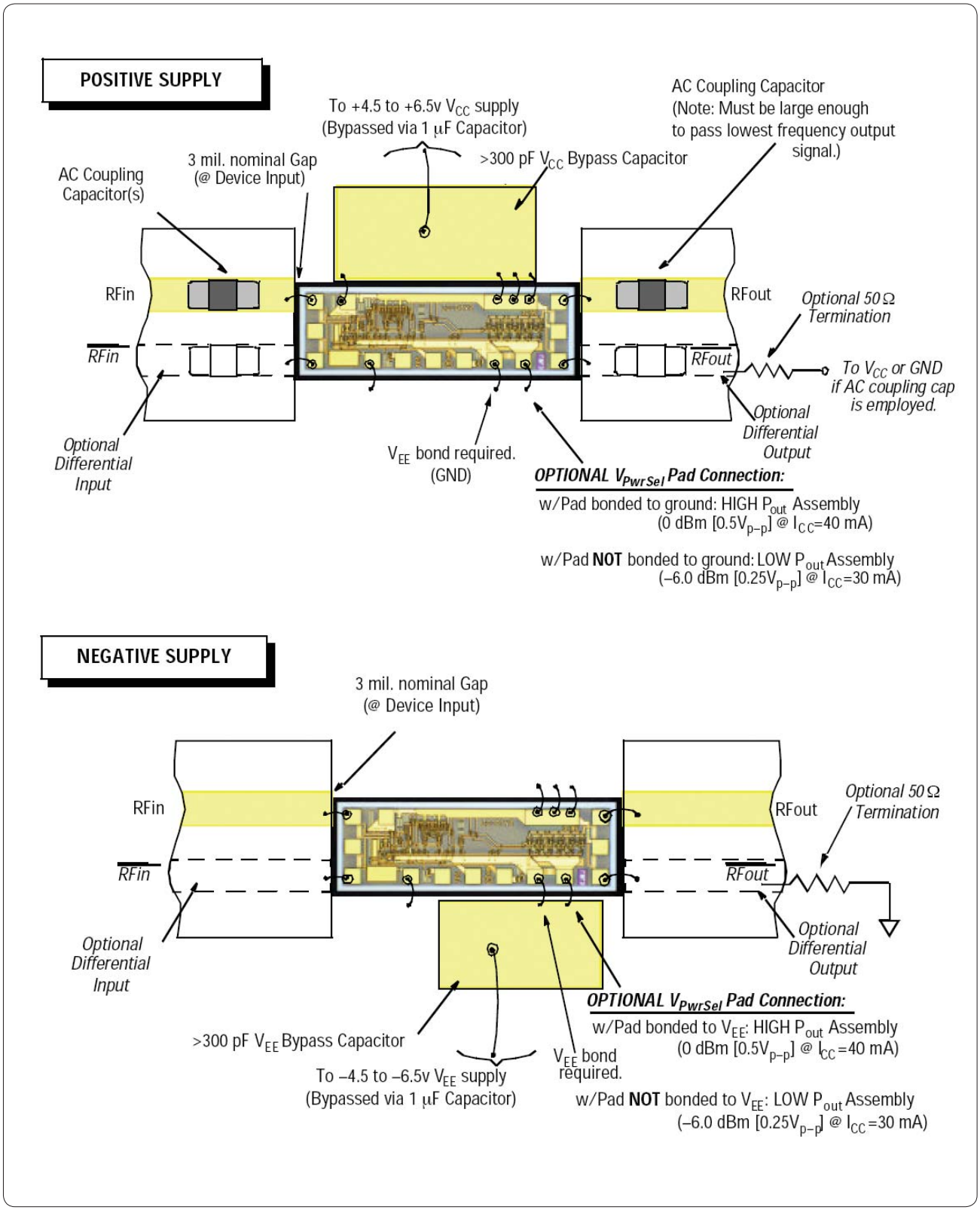


Figure 3. Assembly diagrams

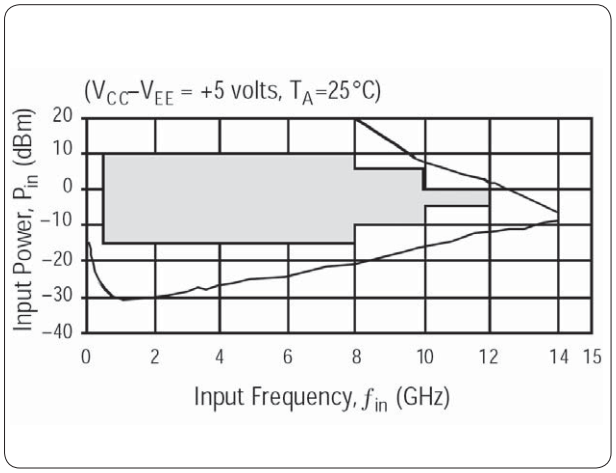


Figure 4. Typical input sensitivity window

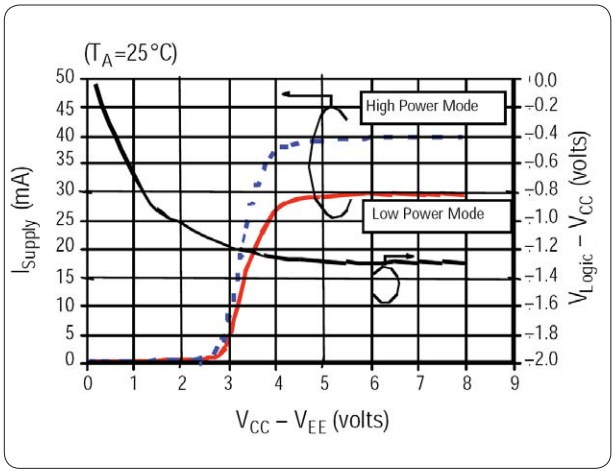


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

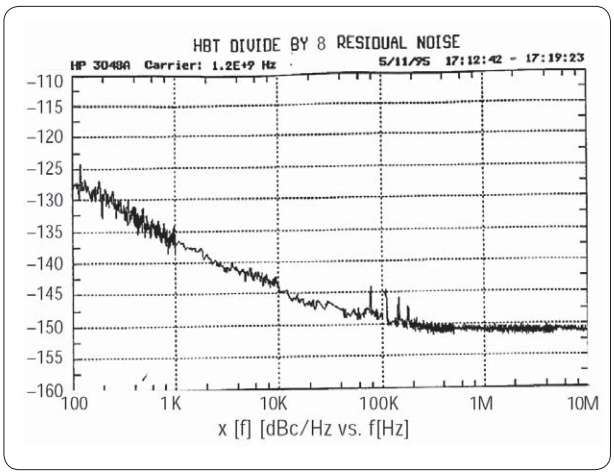


Figure 6. Typical phase noise performance

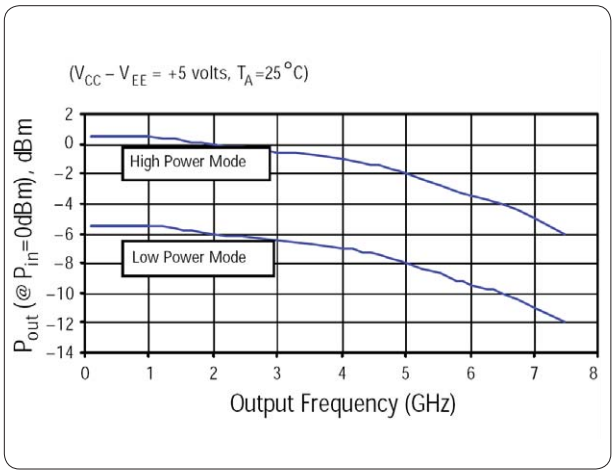


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

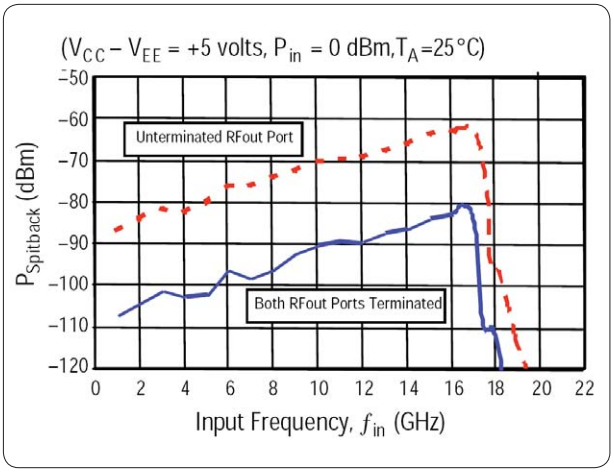


Figure 8. Typical "Spitback" power P(f_{out}) appearing at RF input port

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

LXI

www.lxistandard.org
LXI is the LAN-based successor to GPIB, providing faster, more efficient connectivity. Agilent is a founding member of the LXI consortium.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifi cations. Customers considering the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifi cations from Agilent.
In this data sheet the term typical refers to the 50th percentile performance.
For additional information contact Agilent

MMIC_Helpline@agilent.com.

Remove all doubt

Our repair and calibration services will get your equipment back to you, performing like new, when promised. You will get full value out of your Agilent equipment throughout its lifetime. Your equipment will be serviced by Agilent-trained technicians using the latest factory calibration procedures, automated repair diagnostics and genuine parts. You will always have the utmost confidence in your measurements.

Agilent offers a wide range of additional expert test and measurement services for your equipment, including initial start-up assistance onsite education and training, as well as design, system integration, and project management.

For more information on repair and calibration services, go to:

www.agilent.com/find/removealldoubt

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus
Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

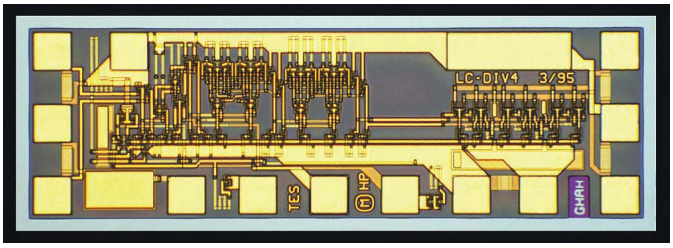
Printed in USA, November 27, 2007
5989-7346EN

Agilent Technologies

Agilent HMMC–3024 DC–12 GHz High Efficiency GaAs HBT MMIC Divide–by–4 Prescaler

1GC1-8007

Data Sheet



Chip Size: 1330 x 440 µm (52.4 x 17.3 mils)
Chip Size Tolerance: ± 10 µm (± 0.4 mils)
Chip Thickness: 127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions: 70 x 70 µm (2.8 x 2.8 mils)

Features

- **Wide Frequency Range: 0.2-12 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -25 to +10 dBm (1–8 GHz) -15 to +18 dBm (8–10 GHz) -10 to +2 dBm (10–12 GHz)**
- **Dual-mode P_{out}: (Chip Form) 0 dBm (0.5 V_{p-p}) @ 40 mA -6.0 dBm (0.25 V_{p-p}) @ 30 mA**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range: 4.5 to 6.5 volt operating range**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-3024 GaAs HBT MMIC prescaler offers dc to 12 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise. In addition to the features listed above the device offers an input disable contact pad to eliminate any self-oscillation condition.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
$V_{Disable}$	Pre-amp disable voltage	V_{EE}	V_{CC}	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ $T_{BS} \leq 85°C$. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

Agilent Technologies

dc Specifications/Physical Properties

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current (**HIGH** Output Power Configuration[2]: $V_{PwrSel} = V_{EE}$)	34	40	46	mA
	Bias supply current (**LOW** Output Power Configuration: V_{PwrSel} = open)	25	30	35	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.32	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.
2. High output power configuration: P_{out} = 0 dBm (V_{out} = 0.5 V_{p-p}). Low output power configuration: P_{out} = -6.0 dBm (V_{out} = 0.25 V_{p-p})

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts) **(÷4)**

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	12	14		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self-Osc.}$	Output Self-Oscillation Frequency[2]		3.4		GHz
P_{in}	@ dc, (Square-wave input)	-15	> -25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	> -20	+10	dBm
	f_{in} = 1 to 8 GHz	-15	> -20	+10	dBm
	f_{in} = 8 to 10 GHz	-10	> -15	+ 5	dBm
	f_{in} = 10 to 12 GHz	-5	> -10	-1	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 10 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 10 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero–crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output edge speed (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave input signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Pre-amp Disable ($V_{Disable}$) feature, or the Differential Input de-biasing technique.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	High Output Power Operating Mode[1] Min.	Typ.	Max.	Units
P_{out}	@ f_{out} < 1 GHz	-2.0	0.0		dBM
	@ f_{out} = 2.5 GHz	-2.5	-0.5		dBm
	@ f_{out} = 3.0 GHz	-3.0	-1.0		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.39	0.5		volts
	@ f_{out} = 2.5 GHz	0.37	0.47		volts
	@ f_{out} = 3.0 GHz	0.35	0.44		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 10 GHz, Unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-53		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, Both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-73		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in}= 0 dBm, referred to P_{in} (f_{in})		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out} (f_{out}))		-25		dBc
		Low Output Power Operating Mode[2]			
P_{out}	@ f_{out} < 1 GHz	-8.0	-6.0		dBm
	@ f_{out} = 2.5 GHz	-8.5	-6.5		dBm
	@ f_{out} = 3.0 GHz	-9.0	-7.0		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.20	0.25		volts
	@ f_{out} = 2.5 GHz	0.19	0.24		volts
	@ f_{out} = 3.0 GHz	0.18	0.22		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 12 GHz, Unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-61		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-82		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in}))		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out} (f_{out}))		-30		dBc

Notes

1. $V_{PwrSel} = V_{EE}$.
2. V_{PwrSel} = Open Circuit.

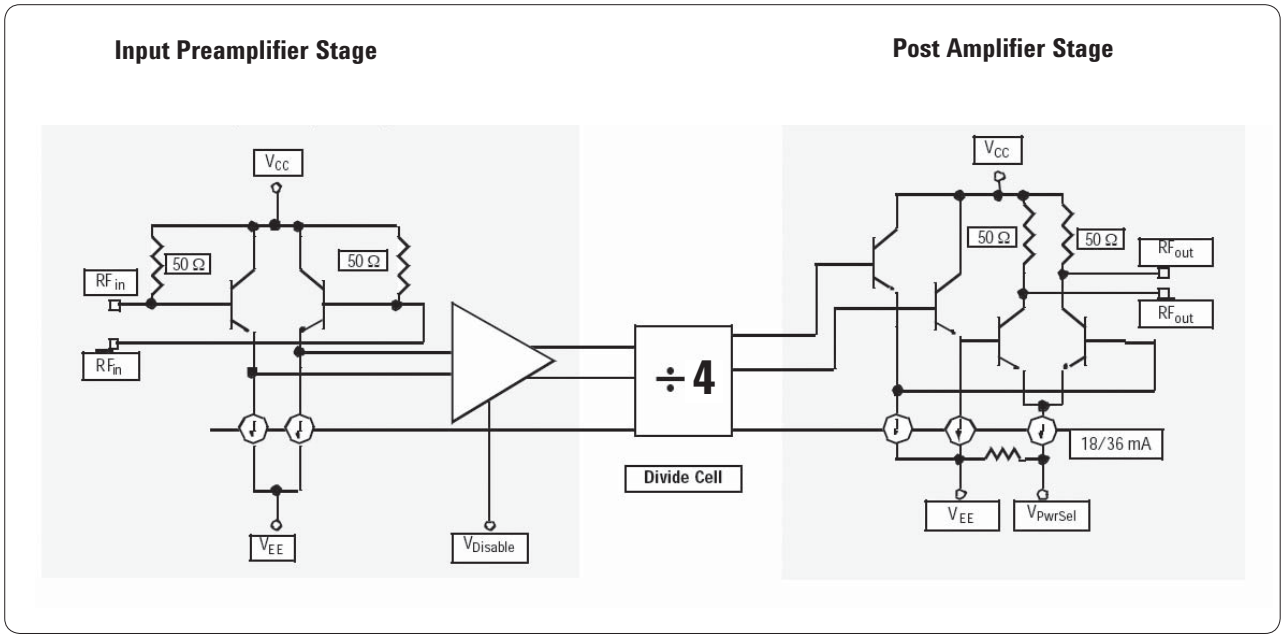


Figure 1. Simplified Schematic

Applications

The HMMC-3024 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 12 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

The device may be biased from either a single positive or single negative supply bias. The backside of the device is not dc connected to any dc bias point on the device.

For positive supply operation V_{CC} is nominally biased at any voltage in the +4.5 to +6.5 volt range with V_{EE} (or V_{EE} & V_{PwrSel}) grounded. For negative bias operation V_{CC} is typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to V_{EE} (or V_{EE} & V_{PwrSel}).

Several features are designed into this prescaler:

1. Dual-Output Power Feature
Bonding both V_{EE} and V_{PwrSel} pads to either ground (positive bias mode) or the negative supply (negative bias mode), will deliver ~0 dBm [0.5 V_{p-p}] at the RF output port while drawing ~40 mA supply current. Eliminating the V_{PwrSel} connection results in reduced output power and voltage swing, -6.0 dBm [0.25 V_{p-p}] but at a reduced current draw of ~30 mA resulting in less overall power dissipation.

(NOTE: V_{EE} must ALWAYS be bonded and V_{PwrSel} must NEVER be biased to any potential other than V_{EE} or open-circuited.)

2. V_{Logic} ECL Contact Pad
Under normal conditions no connection or external bias is required to this pad and it is self-biased to the on-chip ECL logic threshold voltage (V_{CC} -1.35 V). The user can provide an external bias to this pad (1.5 to 1.2 volts less than V_{CC}) to force the prescaler to operate at a system generated logic threshold voltage.

3. Input Disable Feature
If an RF signal with sufficient signal-to-noise ratio is present at the RF input, the prescaler will operate and provide a divided output equal to the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the device may "self-oscillate," especially under small signal input powers or with only noise present at the input. This "self-oscillation" will produce a undesired output signal also known as a false trigger. By applying an external bias to the input disable contact pad (more positive than V_{CC} - 1.35 V), the input preamplifier stage is locked into either logic *"high"* or logic *"low"* preventing frequency division and any self-oscillation frequency which may be present.

4. Input dc Offset
Another method used to prevent false triggers or self-oscillation conditions is to apply a 20 to 100 mV dc offset voltage between the RF_{in} and $\overline{RF}_{in}$ ports. This prevents noise or spurious low level signals from triggering the divider. Adding a 10 KΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ≈25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

Assembly Techniques

Figure 3 shows the chip assembly diagram for single-ended I/O operation through 12 GHz for either positive or negative bias supply operation. In either case the supply contact to the chip must be capacitively bypassed to provide good input sensitivity and low input power feedthrough. Independent of the bias applied to the device, the backside of the chip should always be connected to both a good RF ground plane and a good thermal heat sinking region on the mounting surface.

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not dc grounded, the RF ports should be ac coupled via series capacitors mounted on the thin-film substrate at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the device backside may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

All bonds between the device and this bypass capacitor should be as short as possible to limit the inductance. For operation at frequencies below 1 GHz, a large value capacitor must be added to provide proper RF bypassing.

Due to on-chip 50 Ω matching resistors at all four RF ports, no external termination is required on any unused RF port. However, improved *"Spitback"* performance (~20 dB) and input sensitivity can be achieved by terminating the unused RF_{out} port to V_{CC} through 50 Ω (positive supply) or to ground via a 50 Ω termination (negative supply operation).

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Optional dc Operating Values/Logic Levels

(T_A = 25°C)

Function	Symbol	Conditions	Min (volts/mA)	Typical (volts/mA)	Max (volts/mA)
Logic Threshold[1]	V_{Logic}		V_{CC}-1.45	V_{CC}-1.32	V_{CC}-1.25
Input Disable	$V_{Disable(High)}$ [Disable]		V_{Logic}+0.25	V_{Logic}	V_{CC}
Input Disable	$V_{Disable(Low)}$ [Enable]		V_{EE}	V_{Logic}	V_{Logic}-0.25
Input Disable	$I_{Disable}$	$V_D > V_{EE}$+3	($V_{Disable}$-V_{EE} -3)/500	($V_{Disable}$-V_{EE} -3)/500	($V_{Disable}$-V_{EE} -3)/500
Input Disable	$I_{Disable}$	$V_D < V_{EE}$+3	0	0	0

Note:
1. Acceptable voltage range when applied from external source.

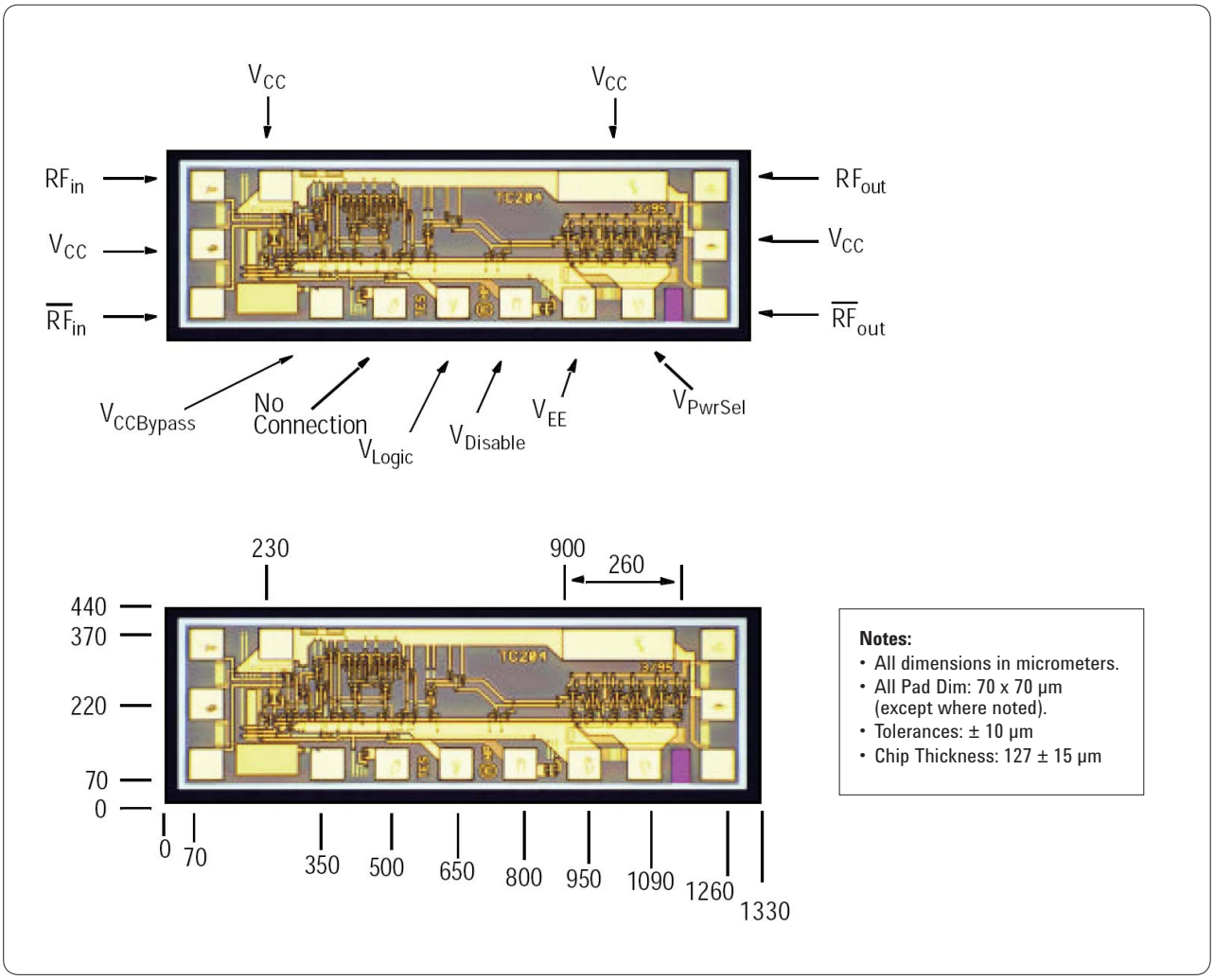


Figure 2. Pad locations and chip dimensions

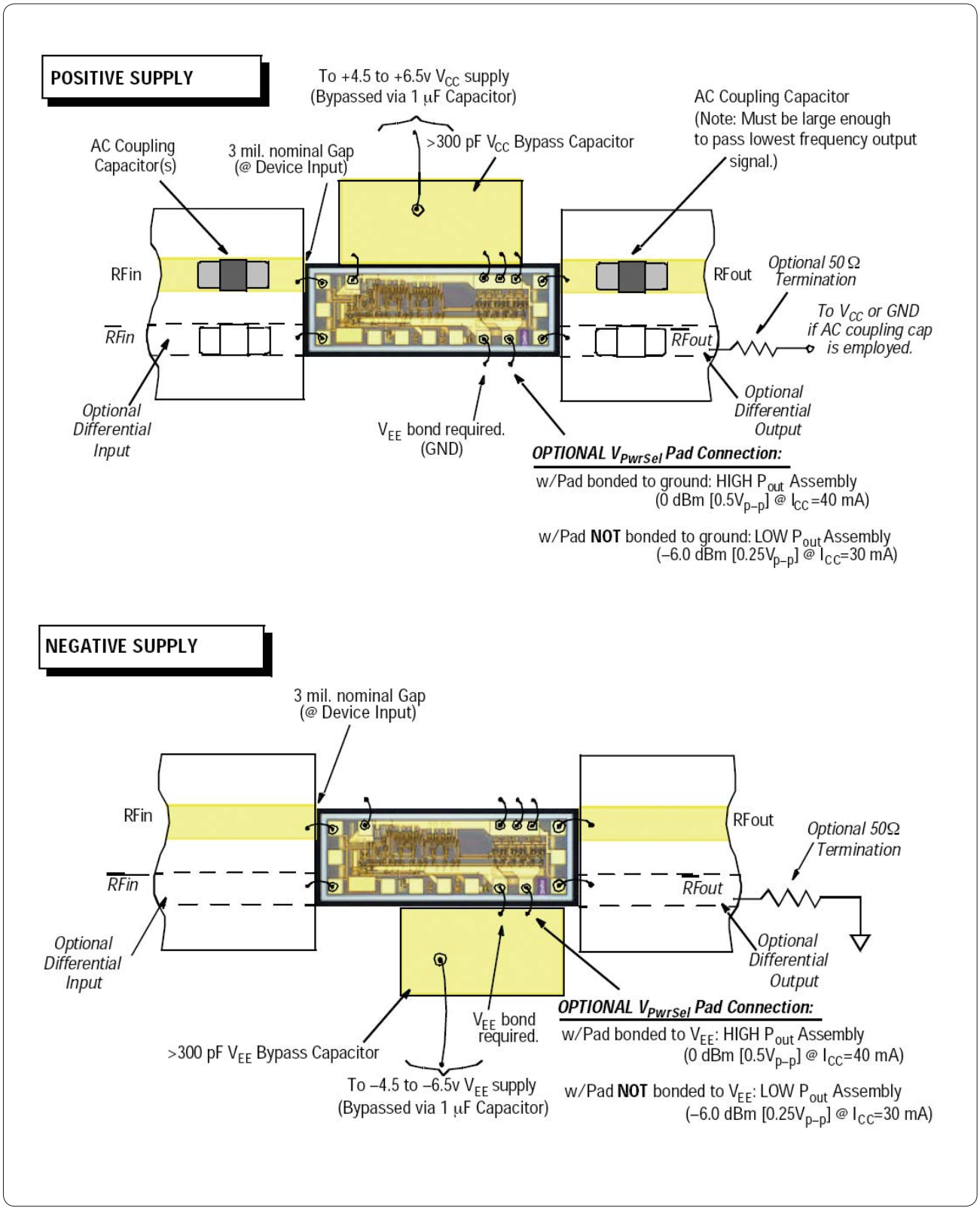


Figure 3. Assembly diagrams

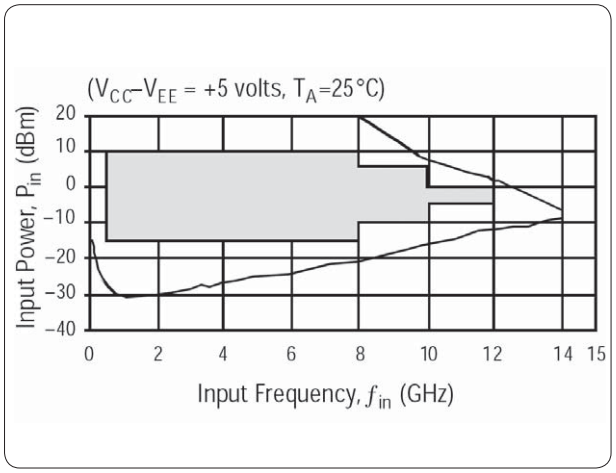


Figure 4. Typical input sensitivity window

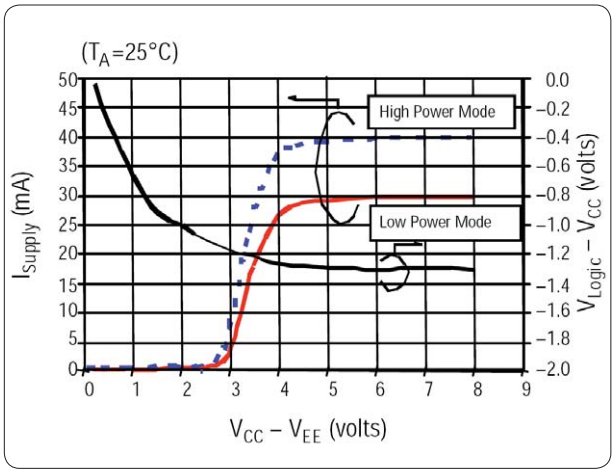


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

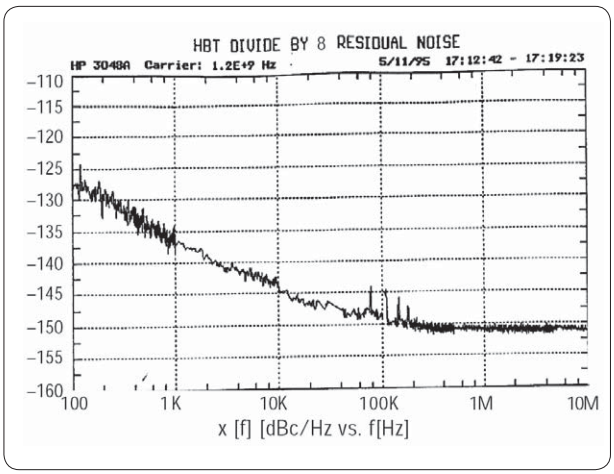


Figure 6. Typical phase noise performance

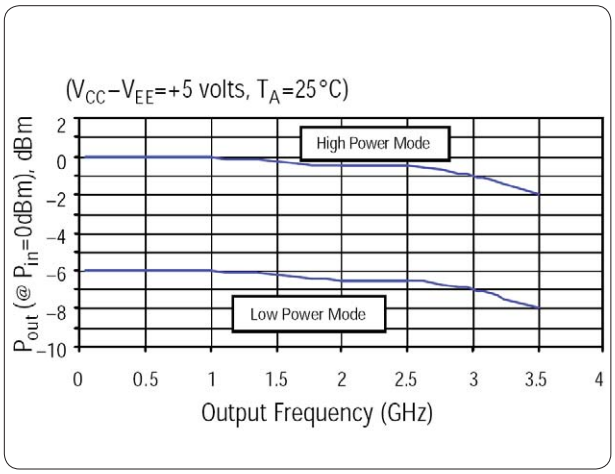


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

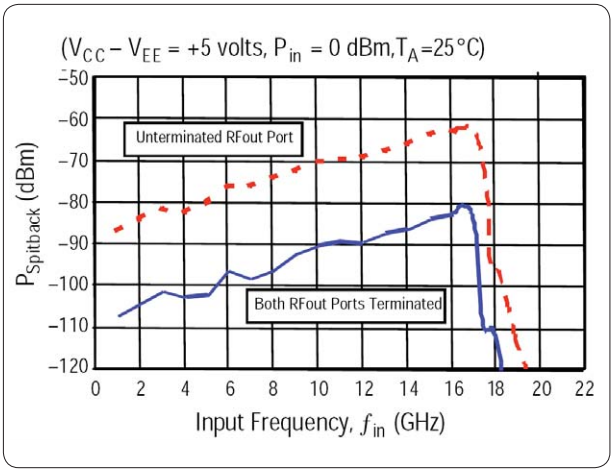


Figure 8. Typical "Spitback" power P(f_{out}) appearing at RF input port

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

LXI

www.lxistandard.org
LXI is the LAN-based successor to GPIB, providing faster, more efficient connectivity. Agilent is a founding member of the LXI consortium.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifi cations. Customers considering the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifi cations from Agilent.
In this data sheet the term typical refers to the 50th percentile performance. For additional information contact Agilent.

MMIC_Helpline@agilent.com.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus
Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

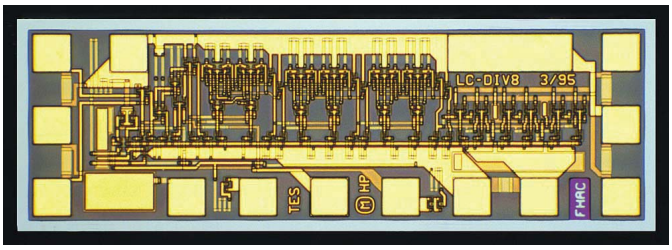
Printed in USA, November 16, 2007
5989-7347EN

Agilent Technologies

Agilent HMMC–3028
DC–12 GHz High Efficiency GaAs HBT MMIC Divide–by–8 Prescaler

1GC1-8008

Data Sheet



Chip Size: 1330 x 440 µm (52.4 x 17.3 mils)
Chip Size Tolerance: ± 10 µm (± 0.4 mils)
Chip Thickness: 127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions: 70 x 70 µm (2.8 x 2.8 mils)

Features

- **Wide Frequency Range: 0.2-12 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -20 to +10 dBm (1–8 GHz) -15 to +10 dBm (8–10 GHz) -10 to +5 dBm (10–12 GHz)**
- **Dual-mode P_{out}: (Chip Form) 0 dBm (0.5 V_{p-p}) @ 44 mA -6.0 dBm (0.25 V_{p-p}) @ 34 mA**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range: 4.5 to 6.5 volt operating range**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-3028 GaAs HBT MMIC Prescaler offers dc to 12 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise. In addition to the features listed above the device offers an input disable contact pad to eliminate any self-oscillation condition.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
$V_{Disable}$	Pre-amp disable voltage	V_{EE}	V_{CC}	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ T_{BS} ≤ 85°C. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

Agilent Technologies

dc Specifications/Physical Properties

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current (**HIGH** Output Power Configuration[2]: $V_{PwrSel} = V_{EE}$)	37	44	51	mA
	Bias supply current (**LOW** Output Power Configuration: V_{PwrSel} = open)	29	34	39	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.32	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.
2. High output power configuration: P_{out} = 0 dBm (V_{out} = 0.5 V_{p-p}). Low output power configuration: P_{out} = -6.0 dBm (V_{out} = 0.25 V_{p-p})

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts) **(÷8)**

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	12	14		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self\text{-}Osc.}$	Output Self-Oscillation Frequency[2]		1.7		GHz
P_{in}	@ dc, (Square-wave input)	-15	> -25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	> -20	+10	dBm
	f_{in} = 1 to 8 GHz	-15	> -20	+10	dBm
	f_{in} = 8 to 10 GHz	-10	> -15	+ 5	dBm
	f_{in} = 10 to 12 GHz	-5	> -10	-1	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 12 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 12 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero–crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output edge speed (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave input signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Pre-amp Disable ($V_{Disable}$) feature, or the Differential Input de-biasing technique.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	High Output Power Operating Mode[1] Min.	Typ.	Max.	Units
P_{out}	@ f_{out} < 1 GHz	-2.0	0		dBM
	@ f_{out} = 1.25 GHz	-2.0	0		dBm
	@ f_{out} = 1.5 GHz	-2.25	-0.25		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.39	0.5		volts
	@ f_{out} = 1.25 GHz	0.39	0.5		volts
	@ f_{out} = 1.5 GHz	0.38	0.48		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-61		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-81		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in}= 0 dBm, referred to P_{in} (f_{in})		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 1.5 GHz, referred to P_{out} (f_{out}))		-30		dBc
		Low Output Power Operating Mode[2]			
P_{out}	@ f_{out} < 1 GHz	-8.0	-6.0		dBm
	@ f_{out} = 1.25 GHz	-8.0	-6.0		dBm
	@ f_{out} = 1.5 GHz	-8.25	-6.25		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.20	0.25		volts
	@ f_{out} = 1.25 GHz	0.20	0.25		volts
	@ f_{out} = 1.5 GHz	0.19	0.24		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 10 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-71		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-91		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in}))		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 1.5 GHz, referred to P_{out} (f_{out}))		-35		dBc

Notes

1. $V_{PwrSel} = V_{EE}$.
2. V_{PwrSel} = Open Circuit.

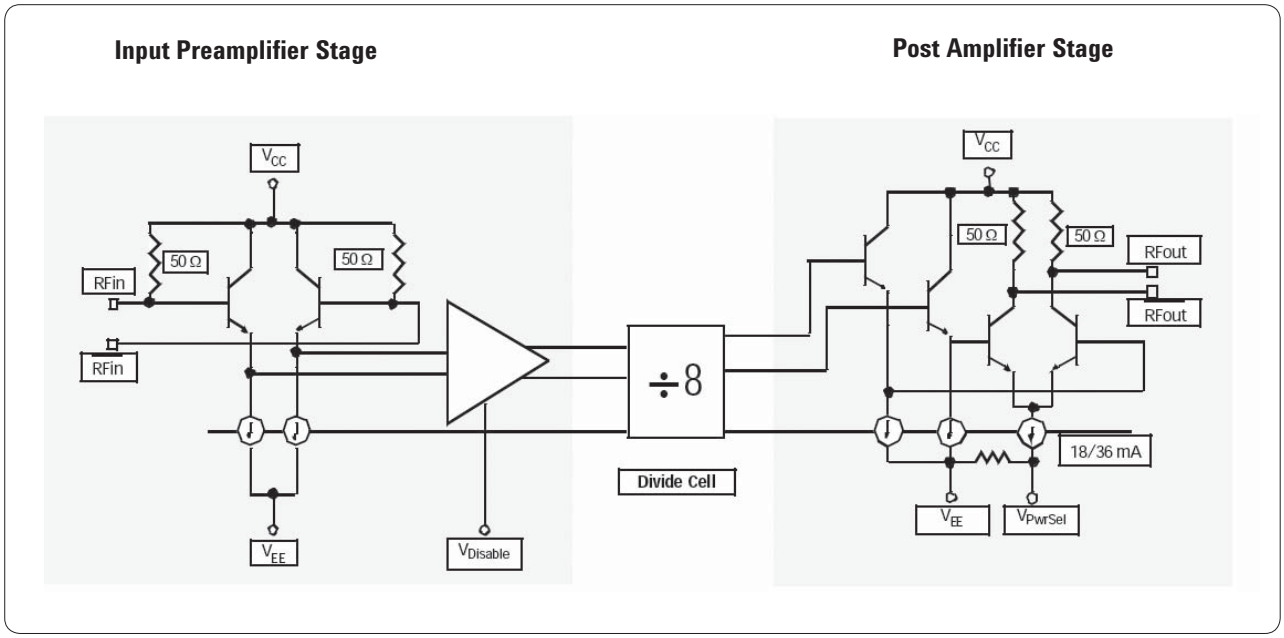


Figure 1. Simplified Schematic

Applications

The HMMC-3028 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 12 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

The device may be biased from either a single positive or single negative supply bias. The backside of the device is not dc connected to any dc bias point on the device.

For positive supply operation V_{CC} is nominally biased at any voltage in the +4.5 to +6.5 volt range with V_{EE} (or V_{EE} & V_{PwrSel}) grounded. For negative bias operation V_{CC} is typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to V_{EE} (or V_{EE} & V_{PwrSel}).

Several features are designed into this prescaler:

1. Dual-Output Power Feature
Bonding both V_{EE} and V_{PwrSel} pads to either ground (positive bias mode) or the negative supply (negative bias mode), will deliver ~0 dBm [0.5 V_{p-p}] at the RF output port while drawing ~40 mA supply current. Eliminating the V_{PwrSel} connection results in reduced output power and voltage swing, -6.0 dBm [0.25 V_{p-p}] but at a reduced current draw of ~30 mA resulting in less overall power dissipation.

(NOTE: V_{EE} must ALWAYS be bonded and V_{PwrSel} must NEVER be biased to any potential other than V_{EE} or open-circuited.)

2. V_{Logic} ECL Contact Pad
Under normal conditions no connection or external bias is required to this pad and it is self-biased to the on-chip ECL logic threshold voltage (V_{CC} -1.35 V). The user can provide an external bias to this pad (1.5 to 1.2 volts less than V_{CC}) to force the prescaler to operate at a system generated logic threshold voltage.

3. Input Disable Feature
If an RF signal with sufficient signal-to-noise ratio is present at the RF input, the prescaler will operate and provide a divided output equal to the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the device may "self-oscillate," especially under small signal input powers or with only noise present at the input. This "self-oscillation" will produce an undesired output signal also known as a false trigger. By applying an external bias to the input disable contact pad (more positive than V_{CC} -1.35 V), the input preamplifier stage is locked into either logic *"high"* or logic *"low"* preventing frequency division and any self-oscillation frequency which may be present.

4. Input dc Offset
Another method used to prevent false triggers or self-oscillation conditions is to apply a 20 to 100 mV dc offset voltage between the RF_{in} and $\overline{RF_{in}}$ ports. This prevents noise or spurious low level signals from triggering the divider.
Adding a 10 KΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ≈25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

Assembly Techniques

Figure 3 shows the chip assembly diagram for single-ended I/O operation through 12 GHz for either positive or negative bias supply operation. In either case the supply contact to the chip must be capacitively bypassed to provide good input sensitivity and low input power feedthrough. Independent of the bias applied to the device, the backside of the chip should always be connected to both a good RF ground plane and a good thermal heat sinking region on the mounting surface.

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not dc grounded, the RF ports should be ac coupled via series capacitors mounted on the thin-film substrate at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the device backside may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

All bonds between the device and this bypass capacitor should be as short as possible to limit the inductance. For operation at frequencies below 1 GHz, a large value capacitor must be added to provide proper RF bypassing.

Due to on-chip 50 Ω matching resistors at all four RF ports, no external termination is required on any unused RF port. However, improved *"Spitback"* performance (~20 dB) and input sensitivity can be achieved by terminating the unused RF_{out} port to V_{CC} through 50 Ω (positive supply) or to ground via a 50 Ω termination (negative supply operation).

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Optional dc Operating Values/Logic Levels

(T_A = 25°C)

Function	Symbol	Conditions	Min (volts/mA)	Typical (volts/mA)	Max (volts/mA)
Logic Threshold[1]	V_{Logic}		V_{CC}-1.5	V_{CC}-1.35	V_{CC}-1.2
Input Disable	$V_{Disable(High)}$ [Disable]		V_{Logic}+0.25	V_{Logic}	V_{CC}
Input Disable	$V_{Disable(Low)}$ [Enable]		V_{EE}	V_{Logic}	V_{Logic}-0.25
Input Disable	$I_{Disable}$	$V_D > V_{EE}$+3	($V_{Disable}$-V_{EE} -3)/500	($V_{Disable}$-V_{EE} -3)/500	($V_{Disable}$-V_{EE} -3)/500
Input Disable	$I_{Disable}$	$V_D < V_{EE}$+3	0	0	0

Note:
1. Acceptable voltage range when applied from external source.

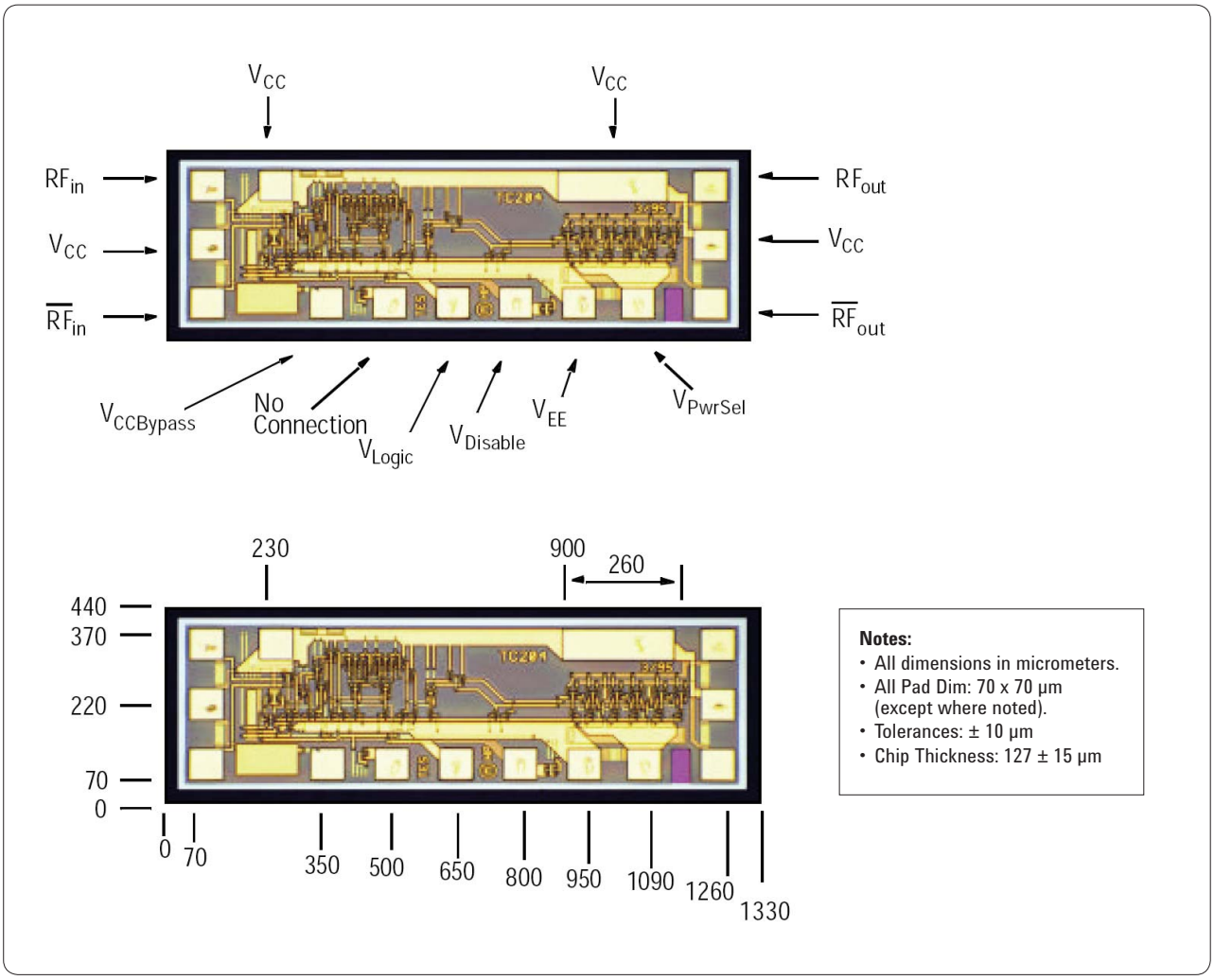


Figure 2. Pad locations and chip dimensions

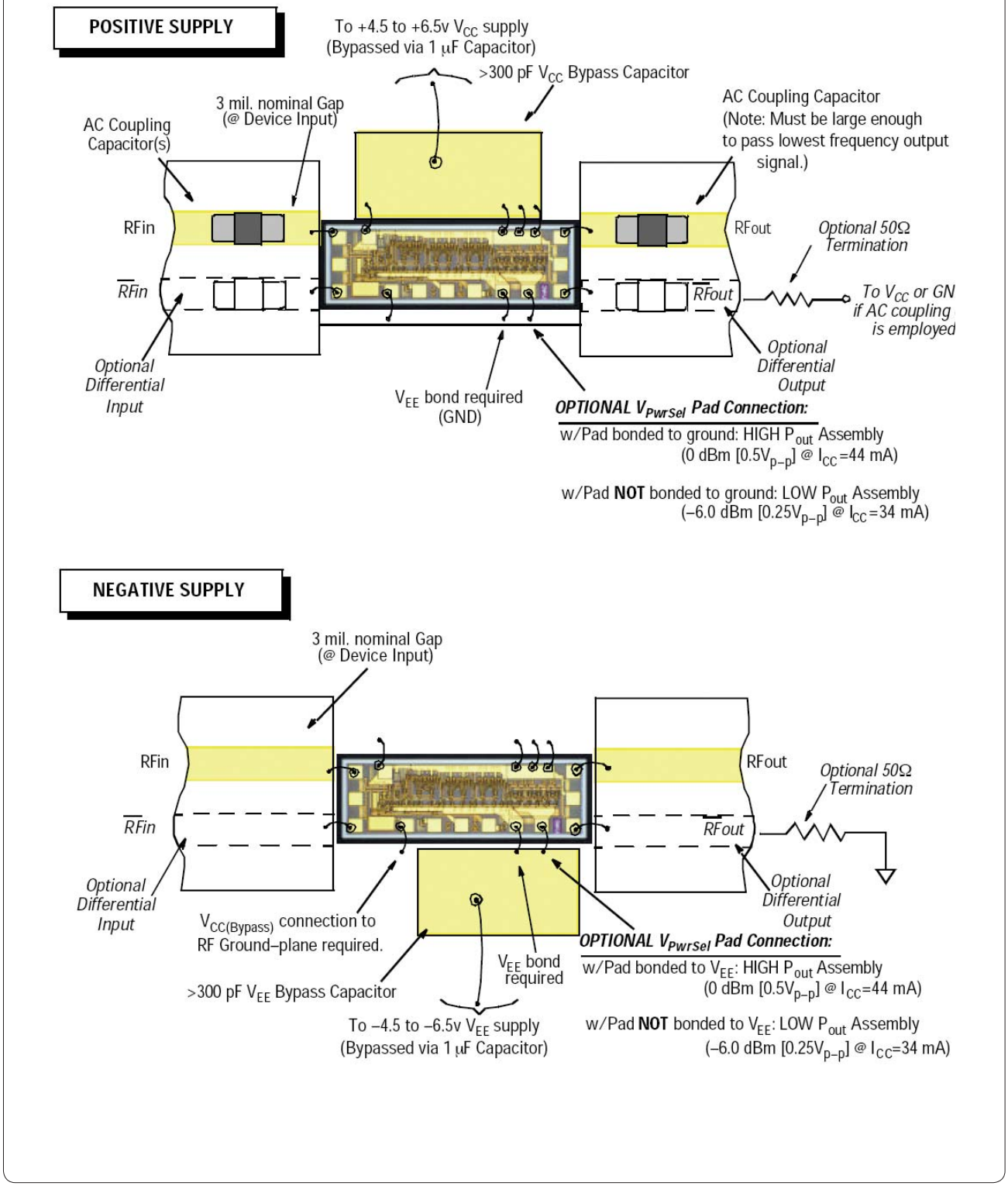


Figure 3. Assembly diagrams

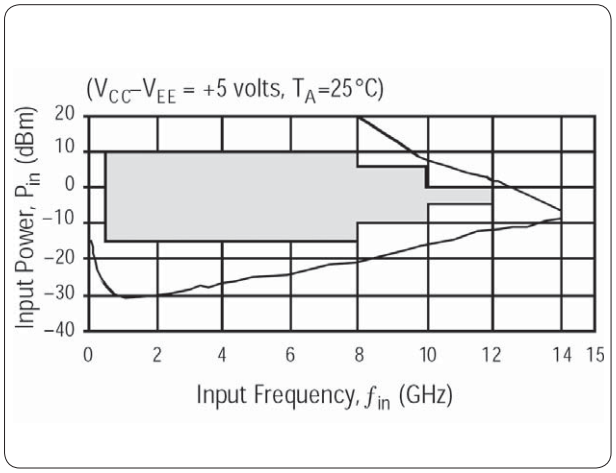


Figure 4. Typical input sensitivity window

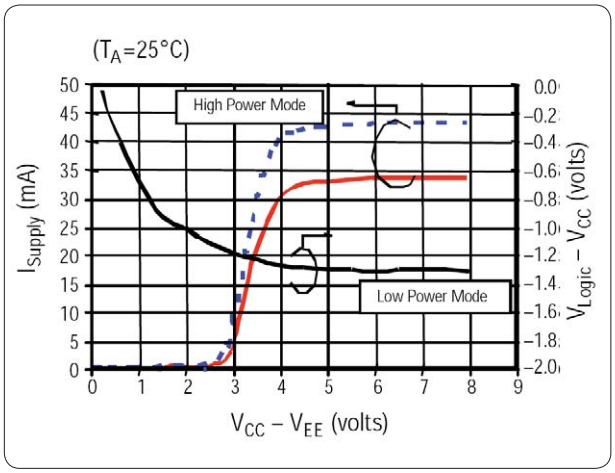


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

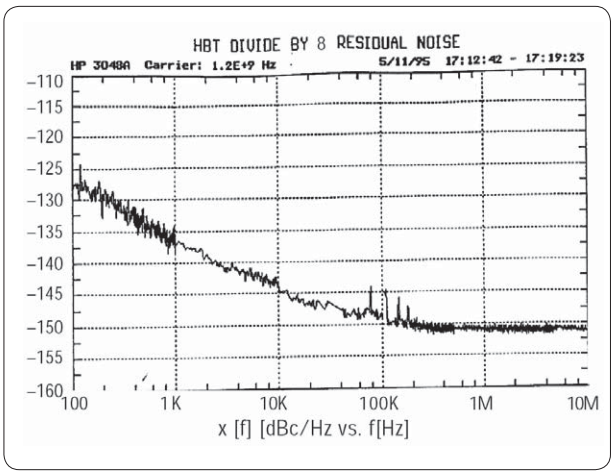


Figure 6. Typical phase noise performance

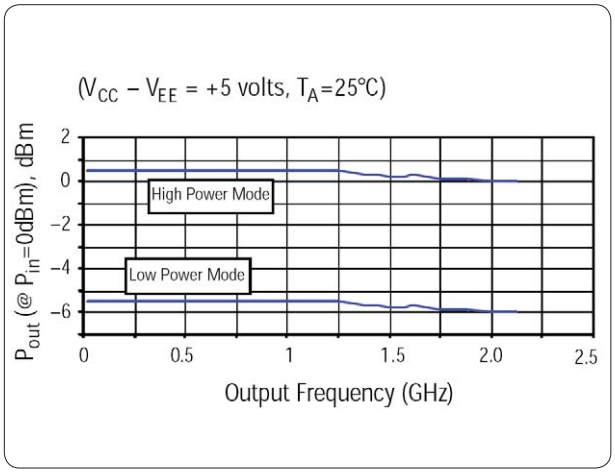


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

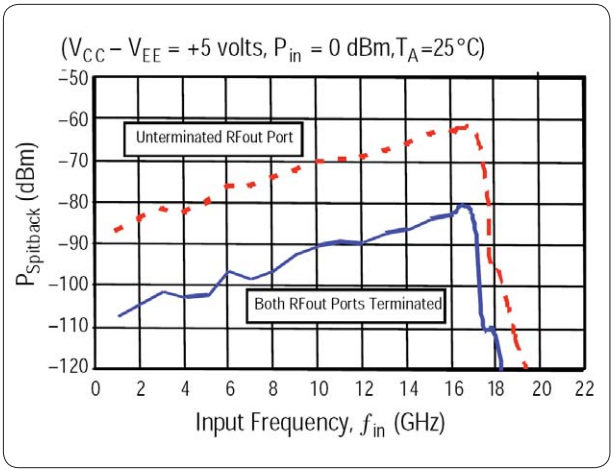


Figure 8. Typical "Spitback" power P(f_{out}) appearing at RF input port

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. Customers considering the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifications from Agilent.
In this data sheet the term typical refers to the 50th percentile performance.
For additional information contact Agilent

MMIC_Helpline@agilent.com.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus

Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

Printed in USA, November 19, 2007
5989-7348EN

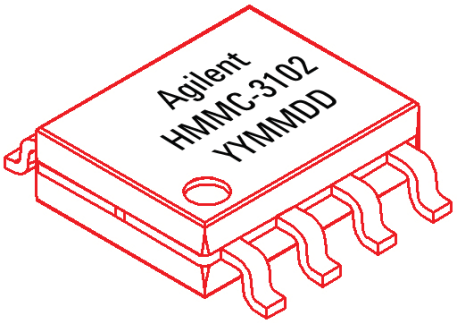
Agilent Technologies

Agilent HMMC-3102 DC-1 GHz Packaged Divide-by-Prescaler

1GC1-8204-TR1-7" diameter reel/500 each

1GC1-8204-BLK-bubble strip/10 each

Data Sheet



Package Type: 8-lead SOIC Plastic
Package Dimensions: 4.9 x 3.9 mm typ.
Package Thickness: 1.55 mm typ.
Lead Pitch: 1.25 mm nom.
Lead Width: 0.42 mm nom.

Features

- **Wide Frequency Range: 0.2-16 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -20 to +10 dBm (1-10 GHz) -15 to +10 dBm (10-12 GHz) -10 to +5 dBm (12-15 GHz)**
- **P_{out}: +6 dBm (0.99 V_{p-p}) will drive ECL**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias with wide range: 4.5 to 6.5 V**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-31 is a packaged GaAs HBT MMIC prescaler which offers dc to 16 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ $T_{BS} \leq 85°C$. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

Agilent Technologies

dc Specifications/Physical Properties

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current	68	80	92	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.35	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	16	18		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self\text{-}Osc.}$	Output Self-Oscillation Frequency[2]		3.4		GHz
P_{in}	@ dc, (Square-wave input)	-15	> -25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	> -20	+10	dBm
	f_{in} = 1 to 10 GHz	-15	> -25	+10	dBm
	f_{in} = 10 to 12 GHz	-10	> -15	+10	dBm
	f_{in} = 12 to 15 GHz	-4	> -10	+4	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 12 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 12 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero–crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output transition time (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave input signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Input dc offset technique described on page 4.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
P_{out}[3]	@ f_{out} < 1 GHz	4	6		dBm
	@ f_{out} = 2.5 GHz	3.5	5,5		dBm
	@ f_{out} = 3.5 GHz	0	2.0		dBm
$\lvert V_{out(p-p)} \rvert$[4]	@ f_{out} < 1 GHz		0.99		volts
	@ f_{out} = 2.5 GHz		0.94		volts
	@ f_{out} = 3.5 GHz		0.63		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 12 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-40		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-47		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 10 GHz, P_{in}= 0 dBm, referred to P_{in} (f_{in}))		-23		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out} (f_{out}))		-25		dBc

Notes

3. Fundamental of output square wave's Fourier Series.
4. Square wave amplitude calculated from P_{out}.

Applications

The HMMC-3102 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 16 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

Due to the presence of an off-chip RF-bypass capacitor inside the package (connected to the V_{CC} contact on the device), and the unique design of the device itself, the component may be biased from either a single positive or single negative supply bias. The backside of the package is not dc connected to any dc bias point on the device.

For positive supply operation, V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with pin 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to pin 8 (V_{EE}).

ac-Coupling and dc-Blocking

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not dc grounded the RF ports should be ac coupled via series capacitors mounted on the PC-board at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the package heat sink may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

Input dc Offset

If an RF signal with sufficient signal to noise ratio is present at the RF input lead, the prescaler will operate and provide a divided output equal the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the component may “self-oscillate”, especially under small signal input powers or with only noise present at the input This “self-oscillation” will produce a undesired output signal also known as a false trigger. To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV dc offset voltage between the RF_{in} and RF_{in} ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 kΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ≈ 25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

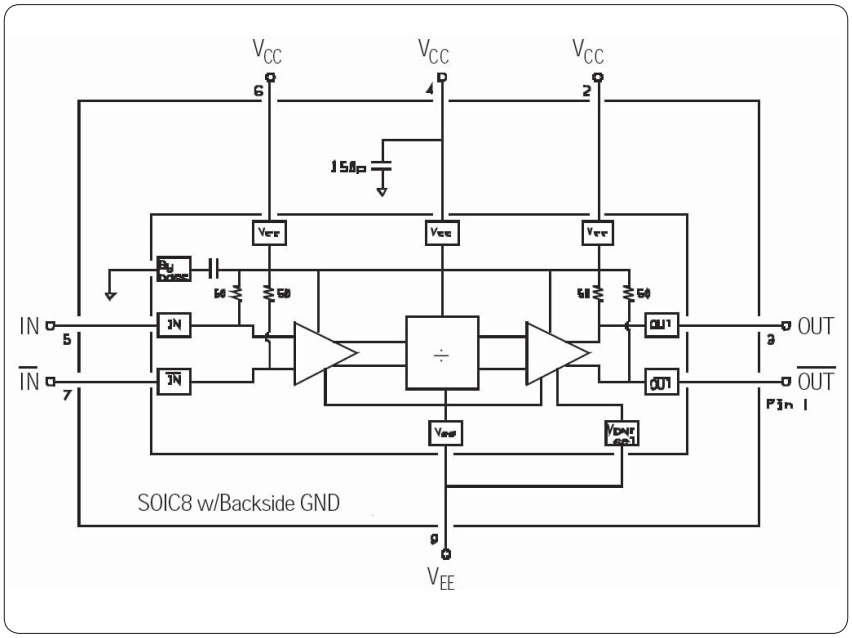


Figure 1. Simplified Schematic

Assembly Notes

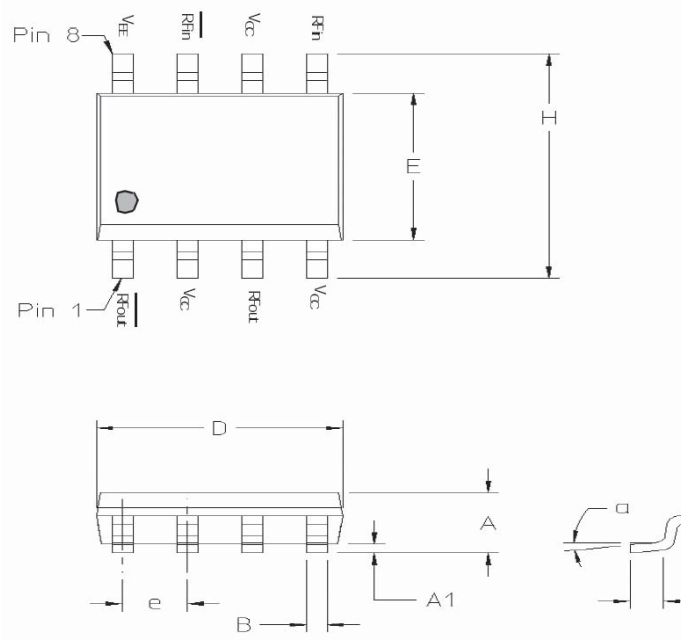
Independent of the bias applied to the package, the backside of the package should always be connected to both a good RF ground plane and a good thermal heat sinking region on the PC board to optimize performance. For single-ended output operation the unused RF output lead should be terminated into 50 Ω to a contact point at the V_{CC} potential or to RF ground through a dc blocking capacitor.

A minimum RF and thermal PC board contact area equal to or greater than 2.67 × 1.65 mm (0.105" × 0.065") with eight 0.020" diameter plated-wall thermal vias is recommended.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Moisture Sensitivity Classification: Class 1, per JESD22-A112-A.



Symbol	Min.	Max.
A	1.35	1.75
A1	0.0	.25
B	0.33	0.51
C	0.19	.025
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	1.27 BSC
H	5.80	6.20
L	0.40	1.27
a	0°	0°

Notes:

- All dimensions in millimeters.
- Refer to JEDEC Outline MS-012 for additional tolerances.
- Exposed heat slug area on package bottom = 2.67 x 1.65.
- Exposed heat sink on package bottom must be soldered to PCB rf ground plane.

Figure 2. Package and dimensions

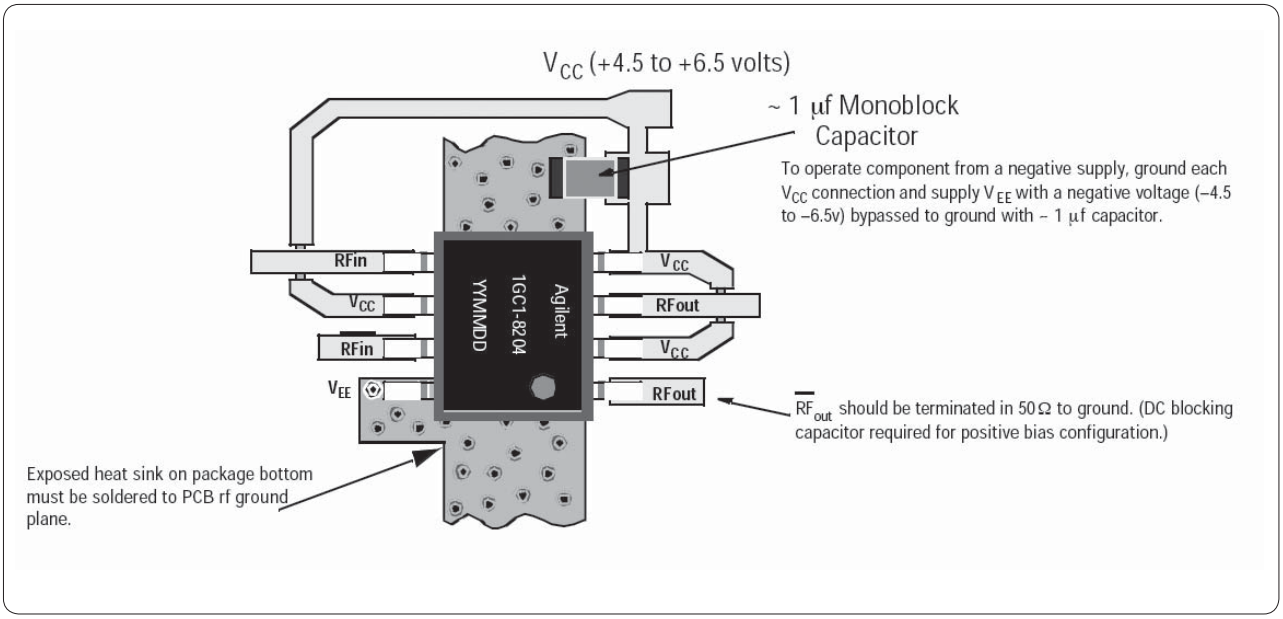


Figure 3. Assembly diagram (single-supply, positive-bias configuration shown)

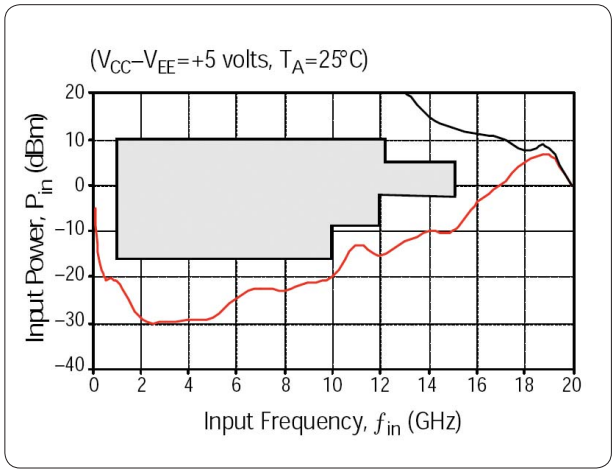


Figure 4. Typical input sensitivity window

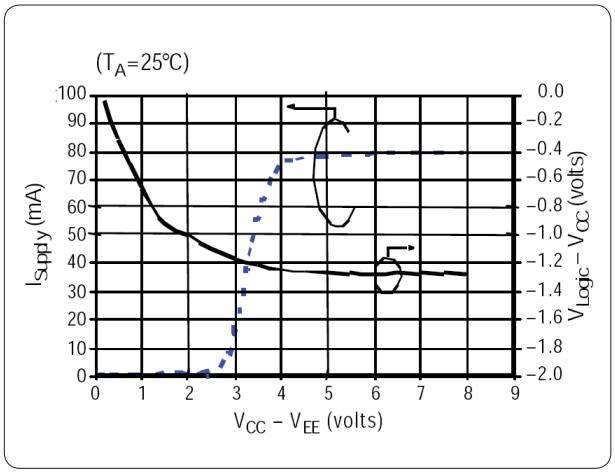


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

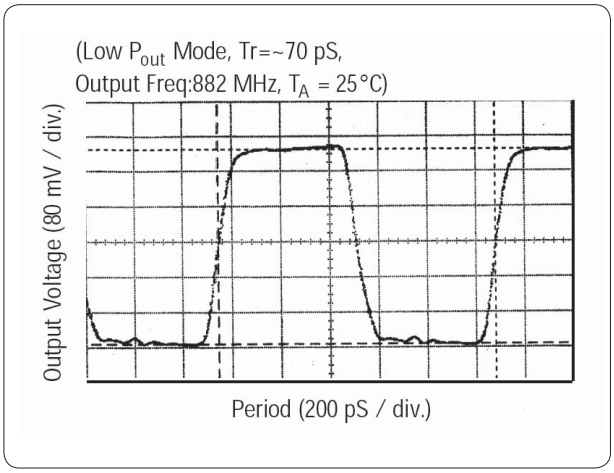


Figure 6. Typical output voltage waveform

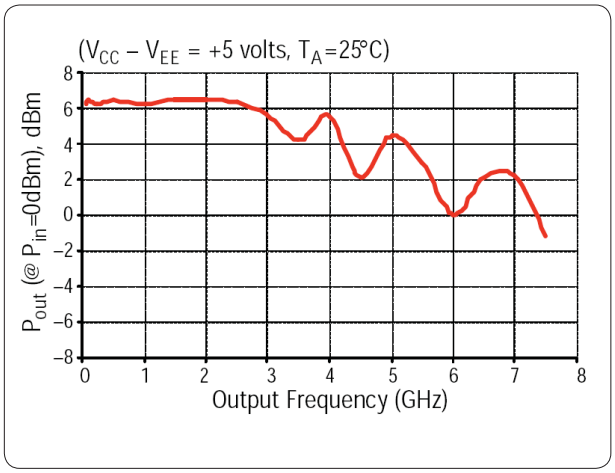


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

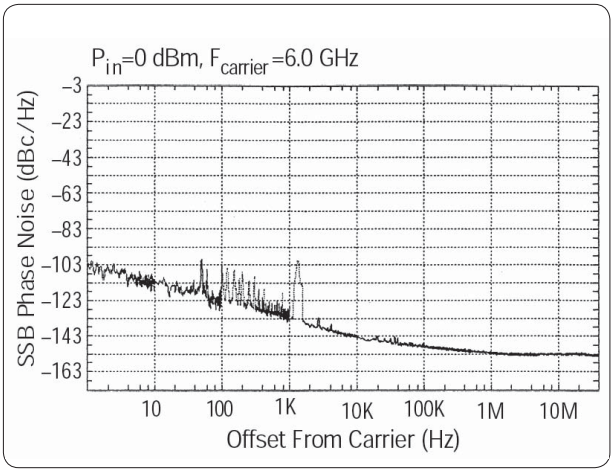


Figure 8. Typical phase noise performance

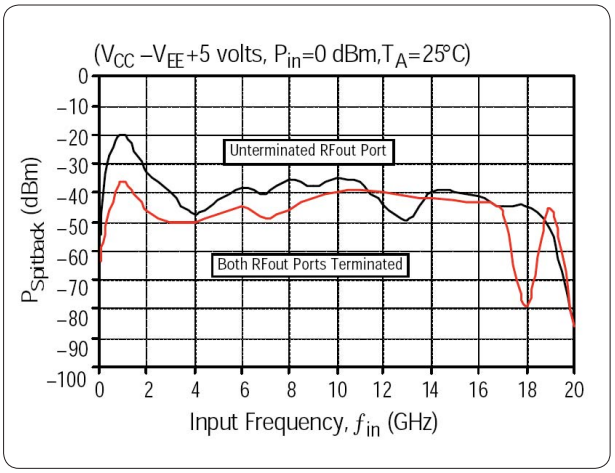
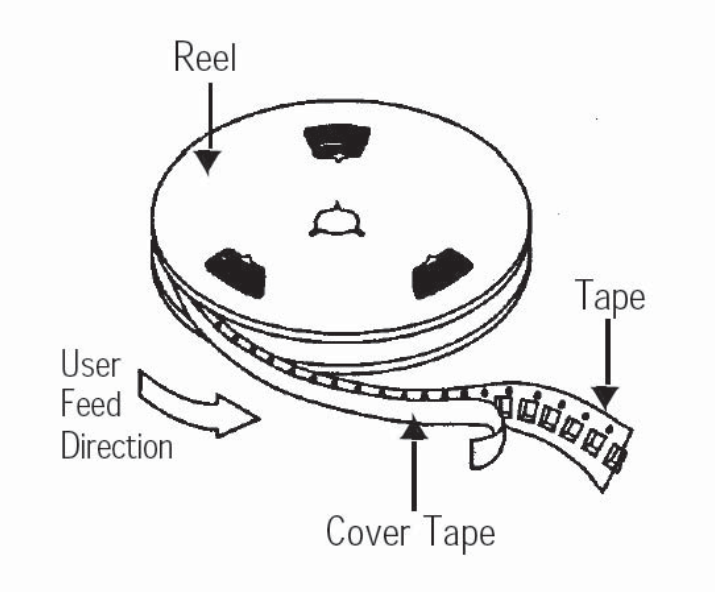
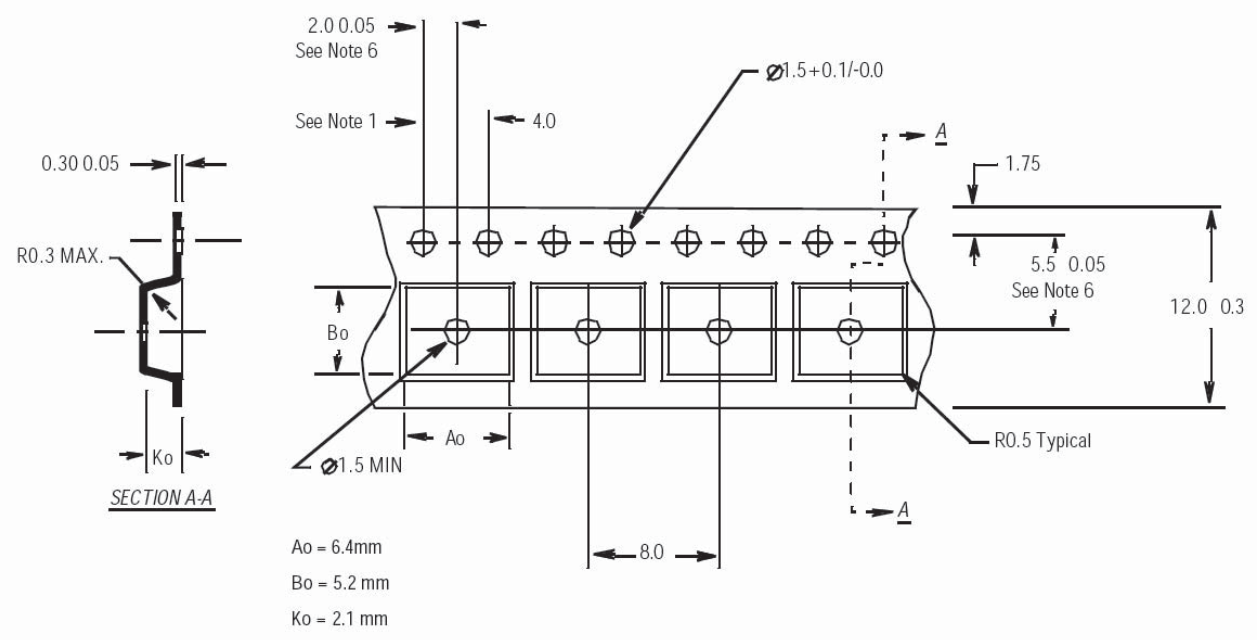


Figure 9. Typical HMMC-3102 "Spitback" power P(f_{out}) appearing at RF input port

Device Orientation



Tape Dimensions and Product Orientation



Notes:

1. 10 sprocket hole pitch cumulative tolerance: 0.2 mm.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3 mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

LXI

www.lxistandard.org
LXI is the LAN-based successor to GPIB, providing faster, more efficient connectivity. Agilent is a founding member of the LXI consortium.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifi cations. Customers considering the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifi cations from Agilent. In this data sheet the term typical refers to the 50th percentile performance. For additional information contact Agilent

MMIC_Helpline@agilent.com.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus
Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

Printed in USA, November 26, 2007
5989-7349EN

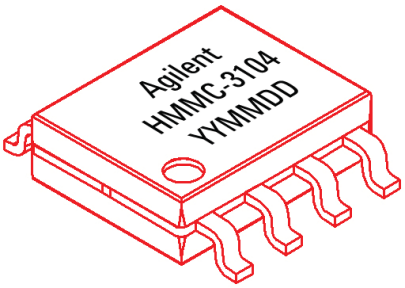
Agilent Technologies

Agilent HMMC-3104 DC-16 GHz Packaged Divide-by-4 Prescaler

1GC1-8202-TR1-7" diameter reel/500 each

1GC1-8202-BLK-bubble strip/10 each

Data Sheet



Package Type:	8-lead SOIC Plastic
Package Dimensions:	4.9 x 3.9 mm typ.
Package Thickness:	1.55 mm typ.
Lead Pitch:	1.25 mm nom.
Lead Width:	0.42 mm nom.

Features

- **Wide Frequency Range: 0.2-16 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -20 to +10 dBm (1-10 GHz) -15 to +10 dBm (10-12 GHz) -10 to +5 dBm (12-15 GHz)**
- **P_{out}: +6 dBm (0.99 V_{p-p}) will drive ECL**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias with wide range: 4.5 to 6.5 V**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-3104 is a packaged GaAs HBT MMIC pre-scaler which offers dc to 16 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	dc input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ $T_{BS} \leq 85°C$. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

Agilent Technologies

DC Specifications/Physical Properties

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current	68	80	92	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.35	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	16	18		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self\text{-}Osc.}$	Output Self-Oscillation Frequency[2]		3.4		GHz
P_{in}	@ dc, (Square-wave input)	-15	> -25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	> -20	+10	dBm
	f_{in} = 1 to 10 GHz	-15	> -25	+10	dBm
	f_{in} = 10 to 12 GHz	-10	> -15	+10	dBm
	f_{in} = 12 to 15 GHz	-4	> -10	+4	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 12 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 12 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero–crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output transition time (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave input signal. Prescaler will operate down to dc for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Input dc offset technique described on page 4.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
P_{out}[3]	@ f_{out} < 1 GHz	4	6		dBm
	@ f_{out} = 2.5 GHz	3.5	5,5		dBm
	@ f_{out} = 3.5 GHz	0	2.0		dBm
$\lvert V_{out(p-p)} \rvert$[4]	@ f_{out} < 1 GHz		0.99		volts
	@ f_{out} = 2.5 GHz		0.94		volts
	@ f_{out} = 3.5 GHz		0.63		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 12 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-40		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-47		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 10 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in}))		-23		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out} (f_{out}))		-25		dBc

Notes

3. Fundamental of output square wave's Fourier Series.
4. Square wave amplitude calculated from P_{out}.

Applications

The HMMC-3104 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 16 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

Due to the presence of an off-chip RF-bypass capacitor inside the package (connected to the V_{CC} contact on the device), and the unique design of the device itself, the component may be biased from either a single positive or single negative supply bias. The backside of the package is not dc connected to any dc bias point on the device.

For positive supply operation, V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with pin 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to pin 8 (V_{EE}).

AC-Coupling and DC-Blocking

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not dc grounded the RF ports should be ac coupled via series capacitors mounted on the PC-board at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the package heat sink may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

Input DC Offset

If an RF signal with sufficient signal to noise ratio is present at the RF input lead, the prescaler will operate and provide a divided output equal the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the component may "self-oscillate", especially under small signal input powers or with only noise present at the input. This "self-oscillation" will produce a undesired output signal also known as a false trigger. To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV dc offset voltage between the RF_{in} and $\overline{RF}_{in}$ ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 kΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ≈ 25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

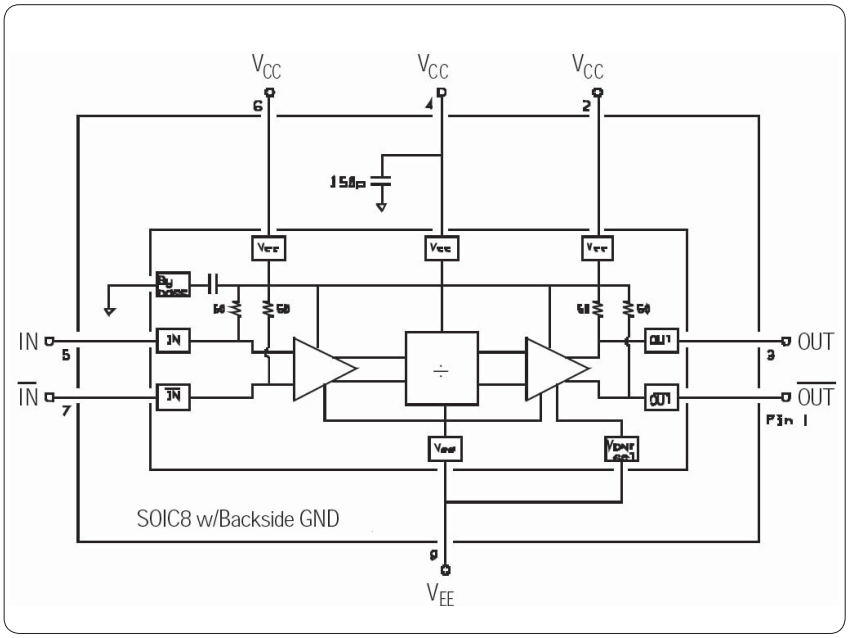


Figure 1. Simplified Schematic

Assembly Notes

Independent of the bias applied to the package, the backside of the package should always be connected to both a good RF ground plane and a good thermal heat sinking region on the PC board to optimize performance. For single-ended output operation the unused RF output lead should be terminated into 50 Ω to a contact point at the V_{CC} potential or to RF ground through a dc blocking capacitor.

A minimum RF and thermal PC board contact area equal to or greater than 2.67 × 1.65 mm (0.105" × 0.065") with eight 0.020" diameter plated-wall thermal vias is recommended.

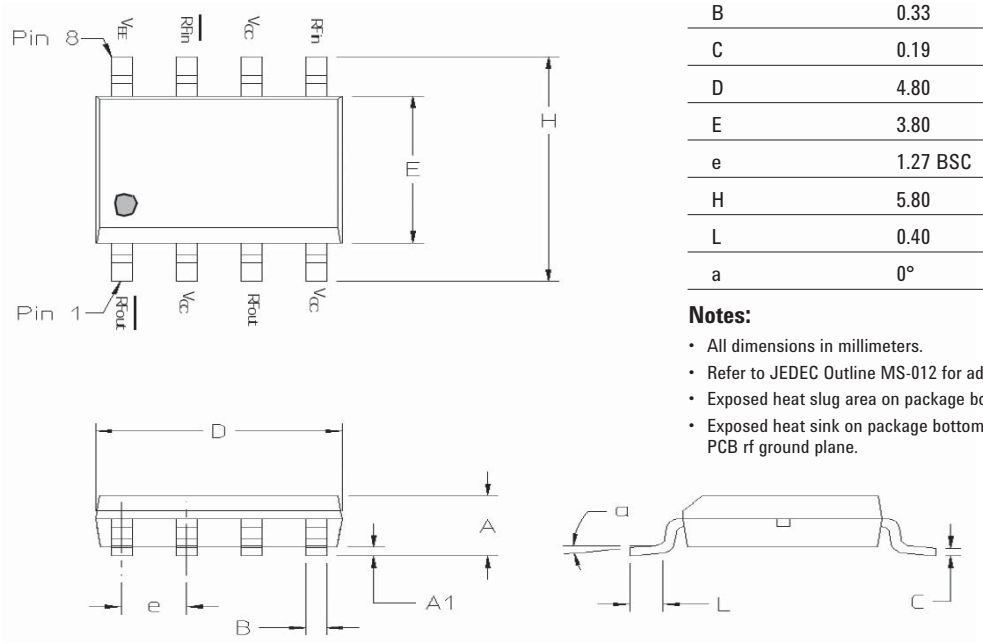
MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Moisture Sensitivity Classification: Class 1, per JESD22-A112-A.

Additional References:

PN #18, "HBT Prescaler Evaluation Board."



Symbol	Min.	Max.
A	1.35	1.75
A1	0.0	.25
B	0.33	0.51
C	0.19	.025
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	1.27 BSC
H	5.80	6.20
L	0.40	1.27
a	0°	0°

Notes:

- All dimensions in millimeters.
- Refer to JEDEC Outline MS-012 for additional tolerances.
- Exposed heat slug area on package bottom = 2.67 x 1.65.
- Exposed heat sink on package bottom must be soldered to PCB rf ground plane.

Figure 2. Package and dimensions

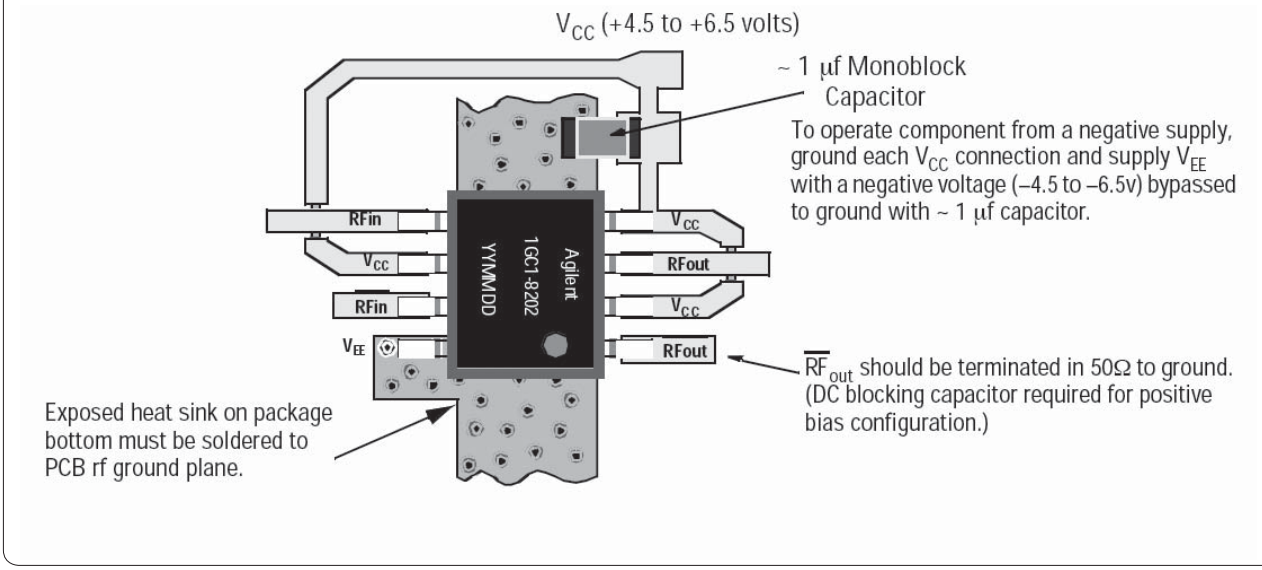


Figure 3. Assembly diagram (Single-supply, positive-bias configuration shown)

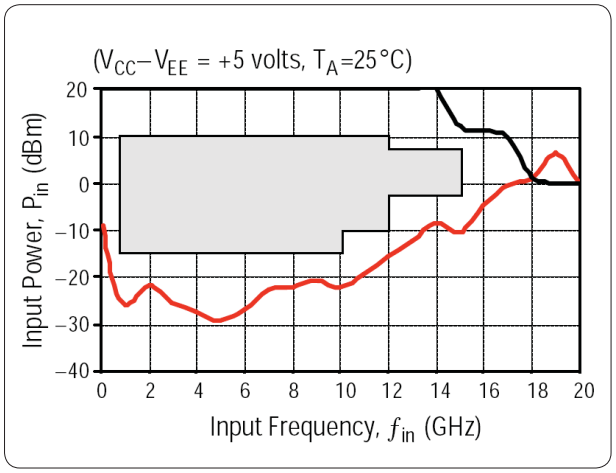


Figure 4. Typical input sensitivity window

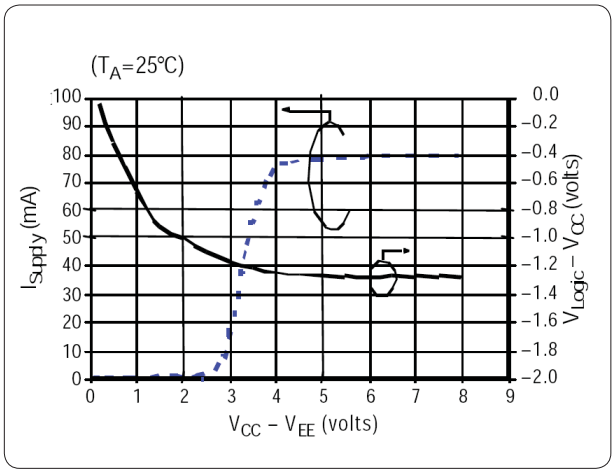


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

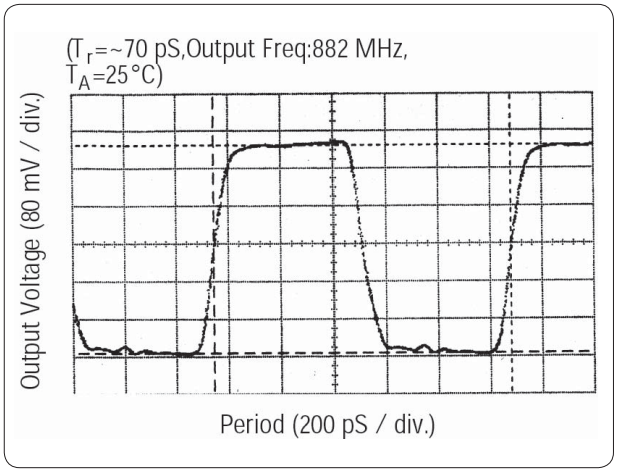


Figure 6. Typical output voltage waveform

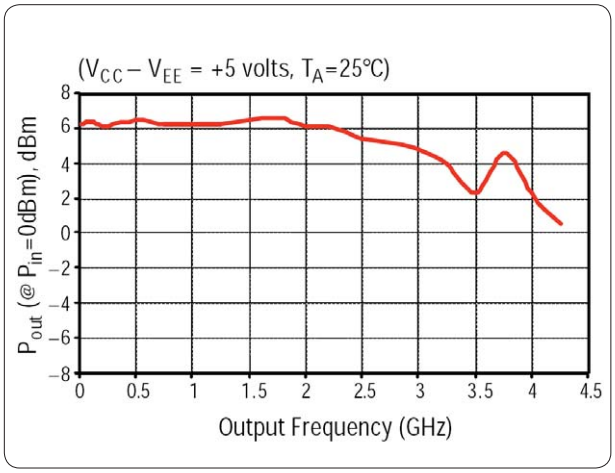


Figure 7. HMMC-3104 output power vs. output frequency, f_{out} (GHz)

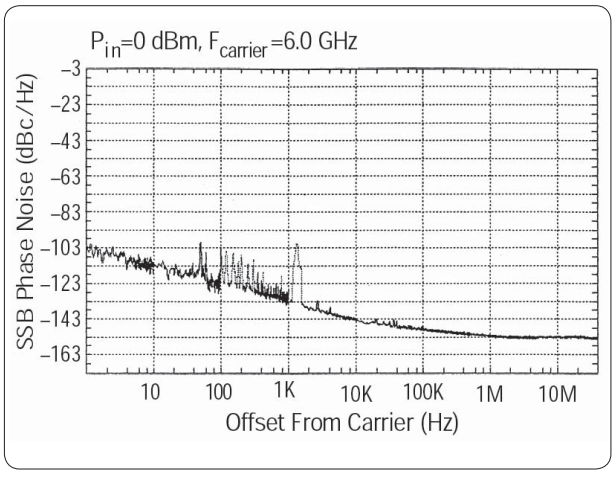


Figure 8. Typical phase noise performance

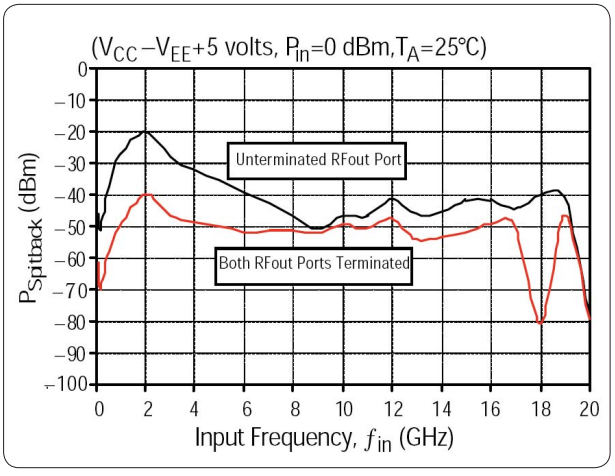
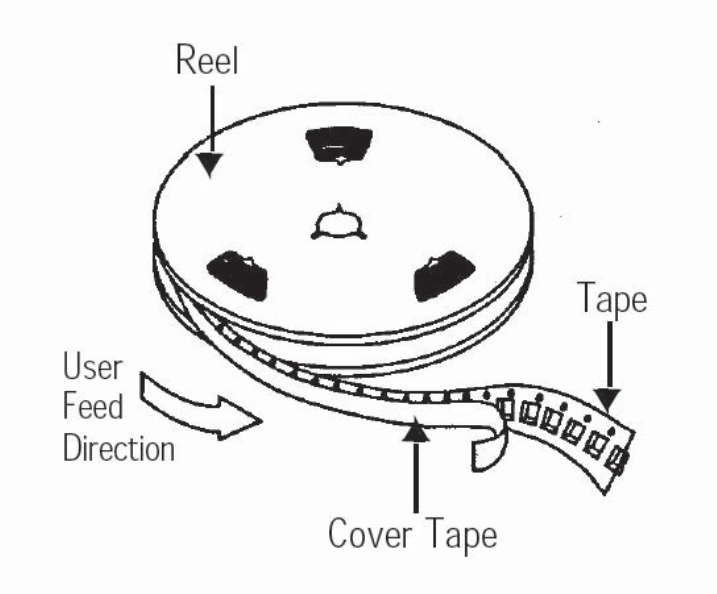
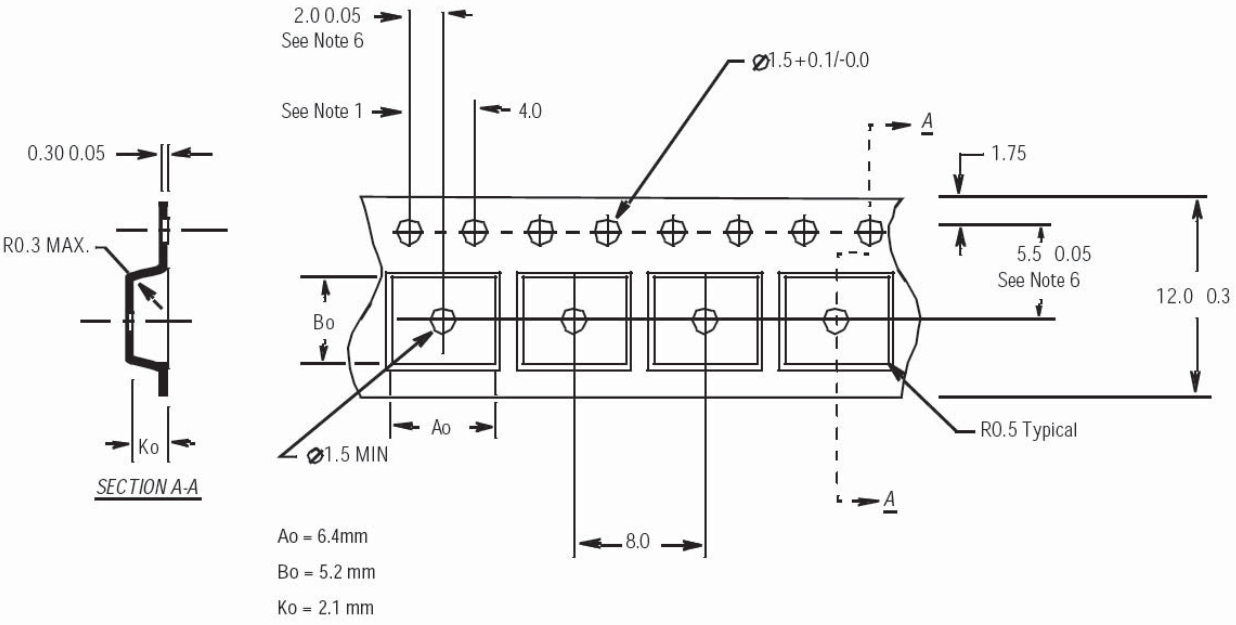


Figure 9. Typical "Spitback" power P(f_{out}) appearing RF input port

Device Orientation



Tape Dimensions and Product Orientation



Notes:

1. 10 sprocket hole pitch cumulative tolerance: 0.2 mm.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3 mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

LXI

www.lxistandard.org
LXI is the LAN-based successor to GPIB, providing faster, more efficient connectivity. Agilent is a founding member of the LXI consortium.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. Customers considering the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifications from Agilent.
In this data sheet the term typical refers to the 50th percentile performance.
For additional information contact Agilent

MMIC_Helpline@agilent.com.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus
Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

Printed in USA, November 26, 2007
5989-7350EN

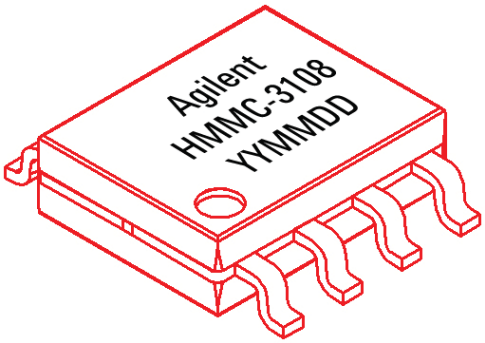
Agilent Technologies

Agilent HMMC-3108 DC-16 GHz Packaged Divide-by-8 Prescaler

1GC1-8203-TR1-7" diameter reel/500 each

1GC1-8203-BLK-bubble strip/10 each

Data Sheet



Package Type:	8-lead SOIC
Package Dimensions:	4.9 x 3.9 mm typ.
Package Thickness:	1.55 mm typ.
Lead Pitch:	1.25 mm nom.
Lead Width:	0.42 mm nom.

Features

- **Wide Frequency Range: 0.2-16 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -20 to +10 dBm (1-10 GHz) -15 to +10 dBm (10-12 GHz) -10 to +5 dBm (12-15 GHz)**
- **P_{out}: +6 dBm (0.99 V_{p-p}) will drive ECL**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation with wide range: 4.5 to 6.5 V**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-3108 is a packaged GaAs HBT MMIC prescaler which offers dc to 16 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ T_{BS} ≤ 85°C. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

DC Specifications/Physical Properties

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current	73	86	99	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.35	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	16	18		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self\text{-}Osc.}$	Output Self-Oscillation Frequency[2]		3.4		GHz
P_{in}	@ dc, (Square-wave input)	-15	> -25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	> -20	+10	dBm
	f_{in} = 1 to 10 GHz	-15	> -25	+10	dBm
	f_{in} = 10 to 12 GHz	-10	> -15	+10	dBm
	f_{in} = 12 to 15 GHz	-4	> -10	+4	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 12 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 12 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero-crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output transition time (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave input signal. Prescaler will operate down to dc for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Input dc offset technique described on page 4.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
P_{out}[3]	@ f_{out} < 1 GHz	4	6		dBm
	@ f_{out} = 2.5 GHz	3.5	5,5		dBm
	@ f_{out} = 3.5 GHz	0	2		dBm
$\lvert V_{out(p-p)} \rvert$[4]	@ f_{out} < 1 GHz		0.99		volts
	@ f_{out} = 2.5 GHz		0.94		volts
	@ f_{out} = 3.5 GHz		0.63		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 12 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-40		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-47		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 10 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in}))		-23		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out} (f_{out}))		-25		dBc

Notes

3. Fundamental of output square wave's Fourier Series.
4. Square wave amplitude calculated from P_{out}.

Applications

The HMMC-3108 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 16 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

Due to the presence of an off-chip RF-bypass capacitor inside the package (connected to the V_{CC} contact on the device), and the unique design of the device itself, the component may be biased from either a single positive or single negative supply bias. The backside of the package is not dc connected to any dc bias point on the device.

For positive supply operation, V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with pin 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to pin 8 (V_{EE}).

AC-Coupling and DC-Blocking

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not dc grounded the RF ports should be ac coupled via series capacitors mounted on the PC-board at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the package heat sink may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

Input DC Offset

If an RF signal with sufficient signal to noise ratio is present at the RF input lead, the prescaler will operate and provide a divided output equal the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the component may "self-oscillate", especially under small signal input powers or with only noise present at the input. This "self-oscillation" will produce a undesired output signal also known as a false trigger. To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV dc offset voltage between the RF_{in} and RF_{in} ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 kΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ≈ 25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

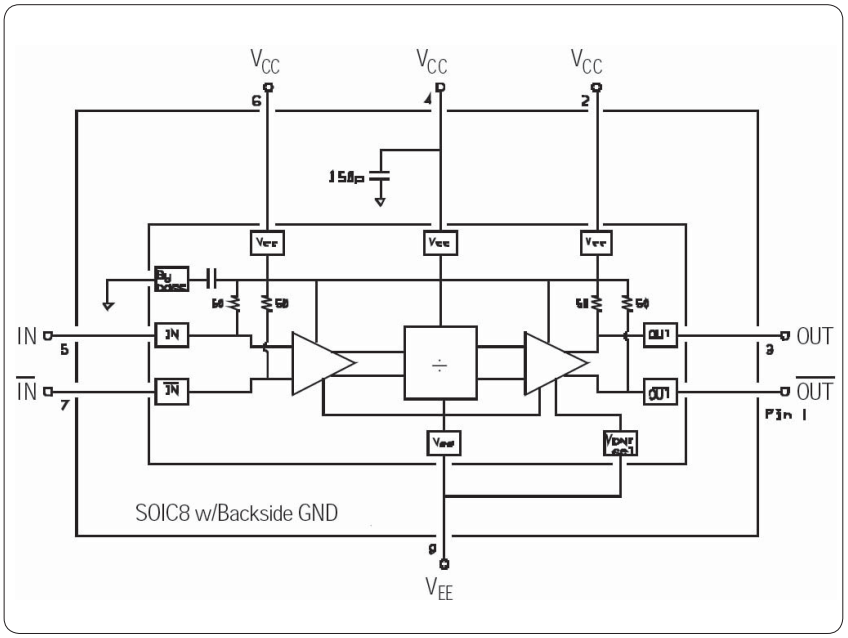


Figure 1. Simplified Schematic

Assembly Notes

Independent of the bias applied to the package, the backside of the package should always be connected to both a good RF ground plane and a good thermal heat sinking region on the PC board to optimize performance. For single-ended output operation the unused RF output lead should be terminated into 50 Ω to a contact point at the V_{CC} potential or to RF ground through a dc blocking capacitor.

A minimum RF and thermal PC board contact area equal to or greater than 2.67 × 1.65 mm (0.105" × 0.065") with eight 0.020" diameter plated-wall thermal vias is recommended.

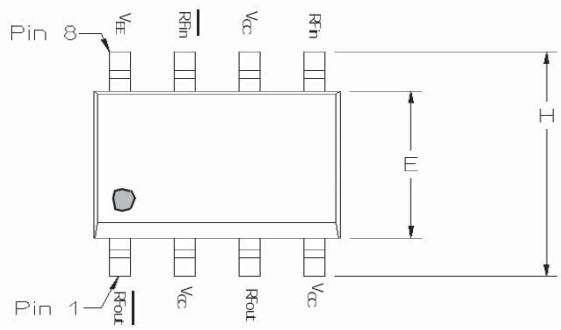
MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

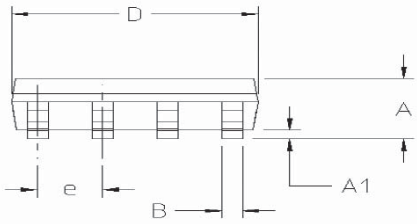
Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

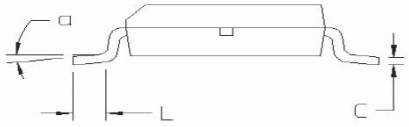
Moisture Sensitivity Classification: Class 1, per JESD22-A112-A.

Additional References:

PN #18, "HBT Prescaler Evaluation Board."







Symbol	Min.	Max.
A	1.35	1.75
A1	0.0	.25
B	0.33	0.51
C	0.19	.025
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	1.27 BSC
H	5.80	6.20
L	0.40	1.27
a	0°	8°

Notes:

- All dimensions in millimeters.
- Refer to JEDEC Outline MS-012 for additional tolerances.
- Exposed heat slug area on package bottom = 2.67 x 1.65.
- Exposed heat sink on package bottom must be soldered to PCB rf ground plane.

Figure 2. Package and dimensions

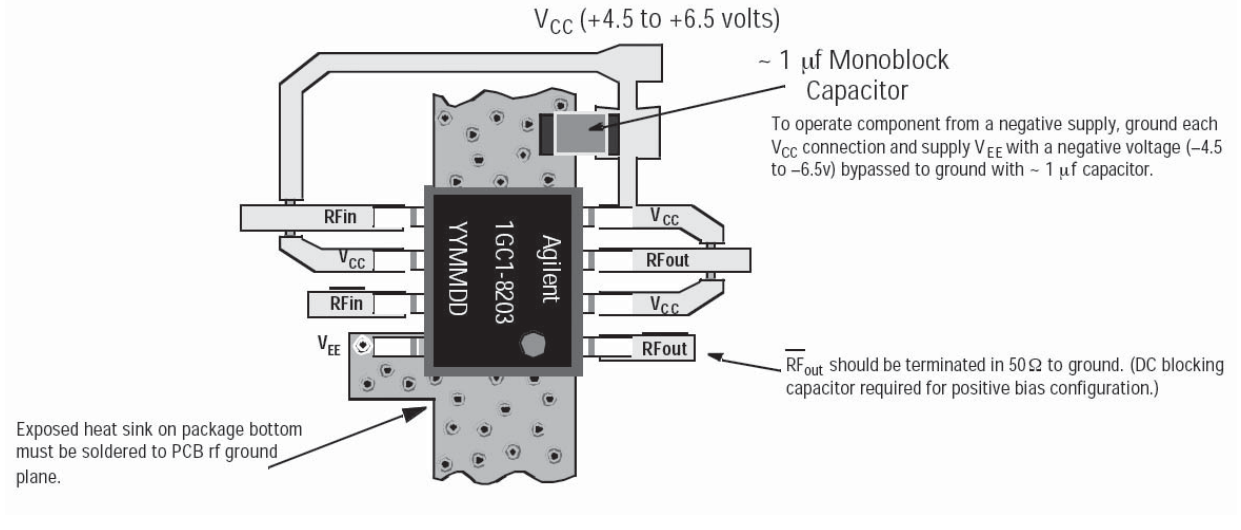


Figure 3. Assembly diagram (Single-supply, positive-bias configuration shown)

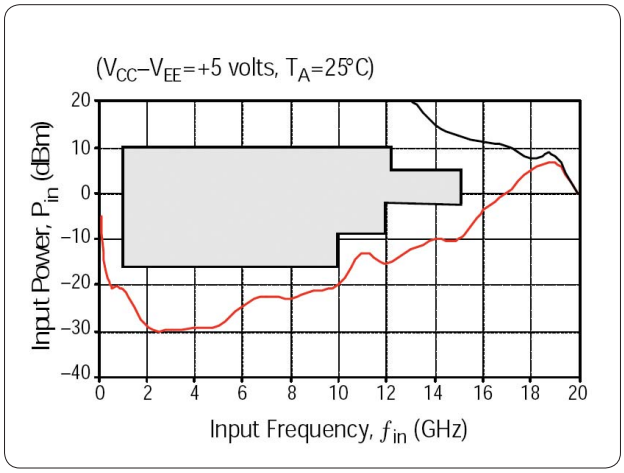


Figure 4. Typical input sensitivity window

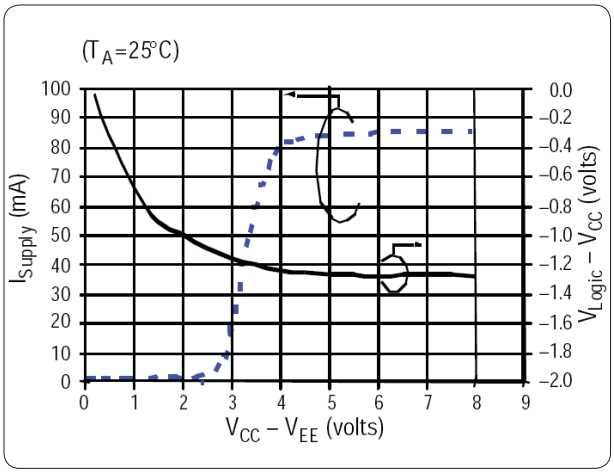


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

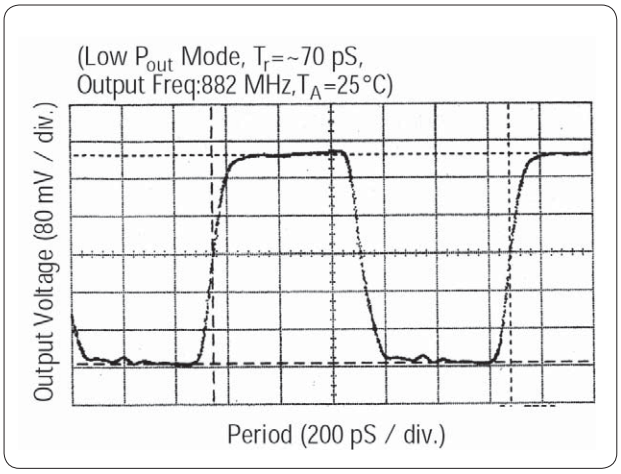


Figure 6. Typical output voltage waveform

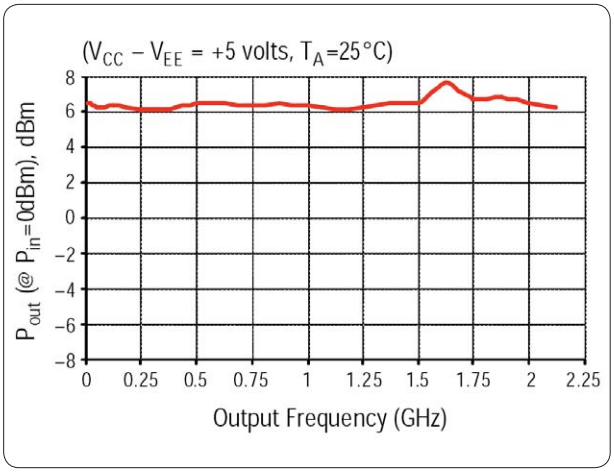


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

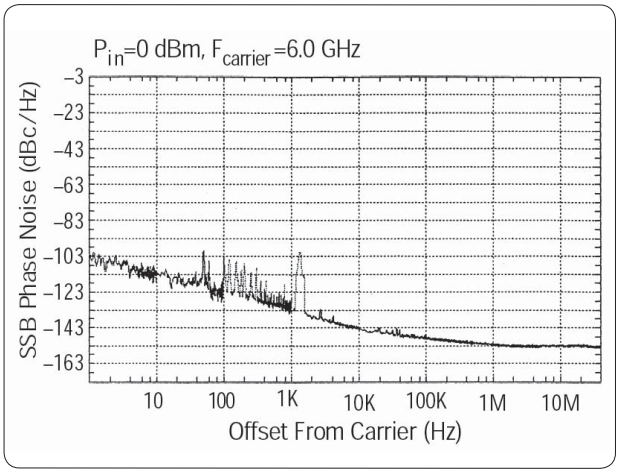


Figure 8. Typical phase noise performance

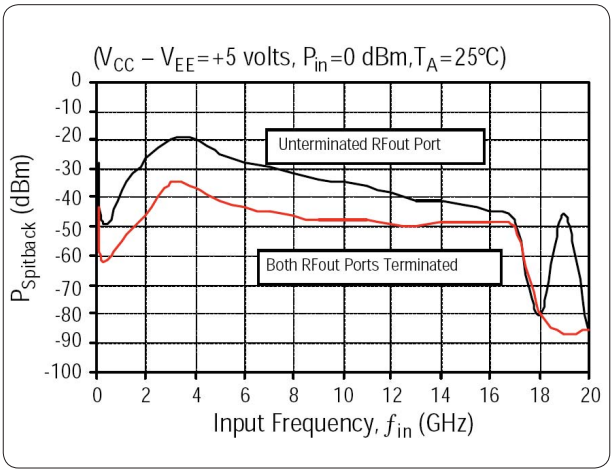
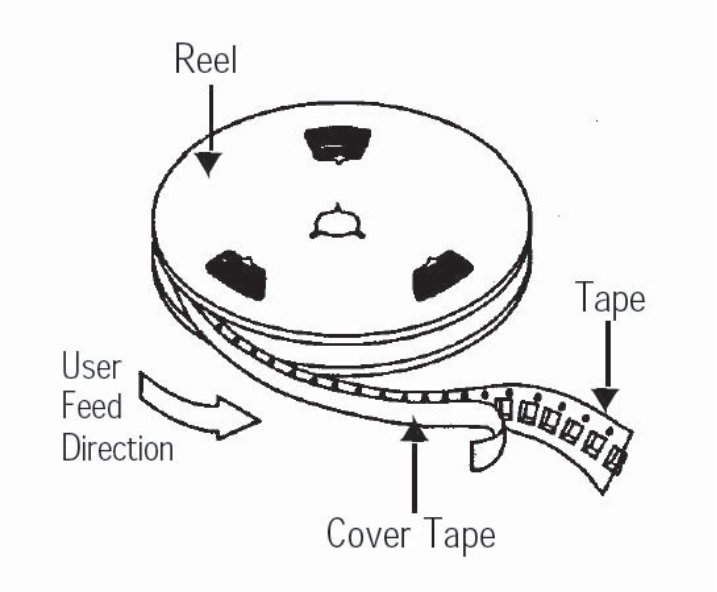
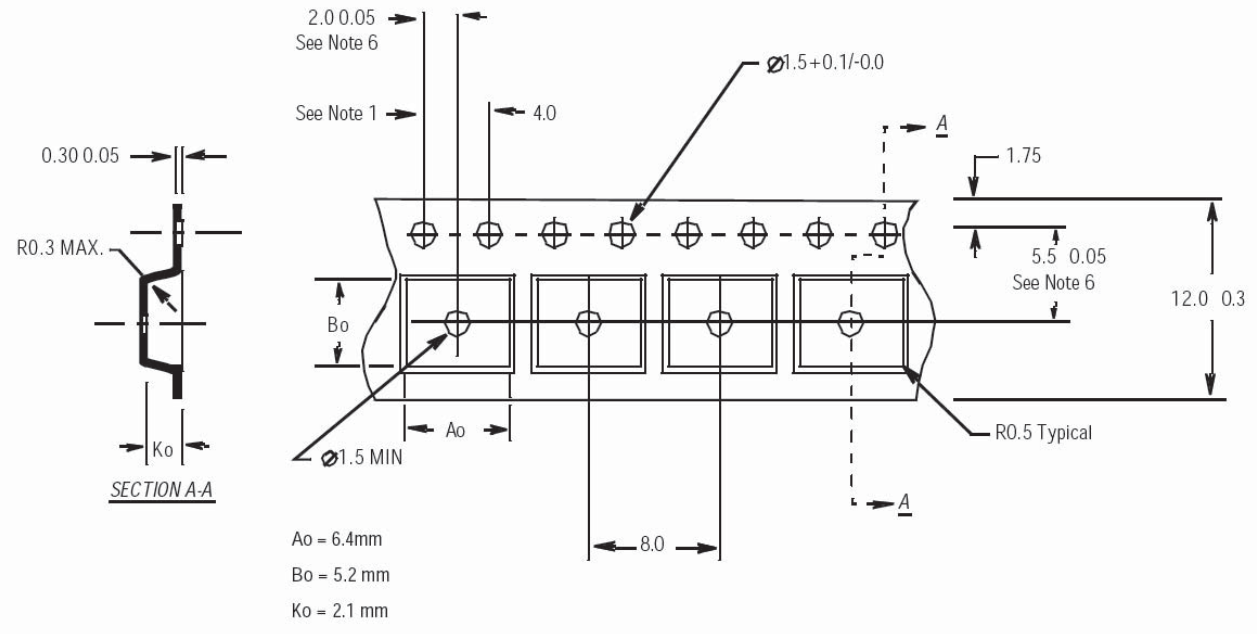


Figure 9. Typical HMMC-3108 "Spitback" power

Device Orientation



Tape Dimensions and Product Orientation



Notes:

1. 10 sprocket hole pitch cumulative tolerance: 0.2 mm.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3 mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

LXI

www.lxistandard.org
LXI is the LAN-based successor to GPIB, providing faster, more efficient connectivity. Agilent is a founding member of the LXI consortium.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifi cations. Customers considering the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifi cations from Agilent. In this data sheet the term typical refers to the 50th percentile performance. For additional information contact Agilent

MMIC_Helpline@agilent.com.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus

Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

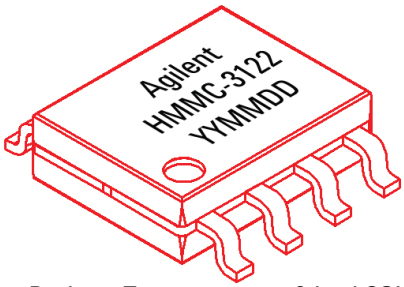
Printed in USA, November 26, 2007
5989-7351EN

Agilent Technologies

Agilent HMMC-3122 DC-12 GHz Packaged High Efficiency Divide-by-2 Prescaler

1GC1-8209-TR1-7" diameter reel/500 each
1GC1-8209-BLK-bubble strip/10 each

Data Sheet



Package Type: 8-lead SOIC Plastic
Package Dimensions: 4.9 x 3.9 mm typ.
Package Thickness: 1.55 mm typ.
Lead Pitch: 1.25 mm nom.
Lead Width: 0.42 mm nom.

Features

- **Wide Frequency Range: 0.2-12 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -15 to +10 dBm (1-8 GHz) -10 to +8 dBm (8-10 GHz) -5 to +2 dBm (10-12 GHz)**
- **P_{out}: 0 dBm (0.5 V_{p-p})**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range: 4.5 to 6.5 volt operating range**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-3122 is a packaged GaAs HBT MMIC pre-scaler which offers dc to 12 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ $T_{BS} \leq 85°C$. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

DC Specifications/Physical Properties

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current	34	40	46	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.32	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	12	14		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self\text{-}Osc.}$	Output Self-Oscillation Frequency[2]		3.4		GHz
P_{in}	@ dc, (Square-wave input)	-15	> -25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	> -20	+10	dBm
	f_{in} = 1 to 8 GHz	-15	> -20	+10	dBm
	f_{in} = 8 to 10 GHz	-10	> -15	+5	dBm
	f_{in} = 10 to 12 GHz	-5	> -10	+1	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 10 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 10 GHz)		30		dB
ϕ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero-crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output transition time (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave input signal. Prescaler will operate down to dc for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Input dc offset technique described on page 4.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
P_{out}[3]	@ f_{out} < 1 GHz	-2	0		dBm
	@ f_{out} = 2.5 GHz	-3.5	-1.5		dBm
	@ f_{out} = 3.0 GHz	-4.5	-2.5		dBm
$\lvert V_{out(p-p)} \rvert$[4]	@ f_{out} < 1 GHz		0.5		volts
	@ f_{out} = 2.5 GHz		0.42		volts
	@ f_{out} = 3.0 GHz		0.37		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 10 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-50		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-55		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in}))		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out} (f_{out}))		-25		dBc

Notes

3. Fundamental of output square wave's Fourier Series.
4. Square wave amplitude calculated from P_{out}.

Applications

The HMMC-3122 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 12 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

Due to the presence of an off-chip RF-bypass capacitor inside the package (connected to the V_{CC} contact on the device), and the unique design of the device itself, the component may be biased from either a single positive or single negative supply bias. The backside of the package is not dc connected to any dc bias point on the device.

For positive supply operation, V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with pin 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to pin 8 (V_{EE}).

AC-Coupling and DC-Blocking

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not dc grounded the RF ports should be ac coupled via series capacitors mounted on the PC board at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the package heat sink may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

Input DC Offset

If an RF signal with sufficient signal to noise ratio is present at the RF input lead, the prescaler will operate and provide a divided output equal the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the component may "self-oscillate", especially under small signal input powers or with only noise present at the input. This "self-oscillation" will produce a undesired output signal also known as a false trigger. To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV dc offset voltage between the RF_{in} and RF_{in} ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 kΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ≈ 25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

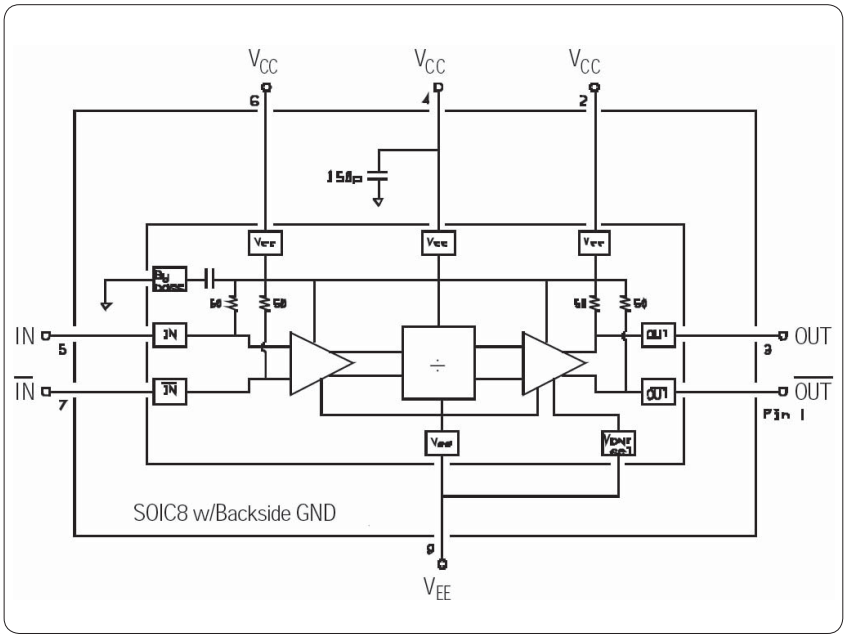


Figure 1. Simplified Schematic

Assembly Notes

Independent of the bias applied to the package, the backside of the package should always be connected to both a good RF ground plane and a good thermal heat sinking region on the PC board to optimize performance. For single-ended output operation the unused RF output lead should be terminated into 50 Ω to a contact point at the V_{CC} potential or to RF ground through a dc blocking capacitor.

A minimum RF and thermal PC board contact area equal to or greater than 2.67 × 1.65 mm (0.105" × 0.065") with eight 0.020" diameter plated-wall thermal vias is recommended.

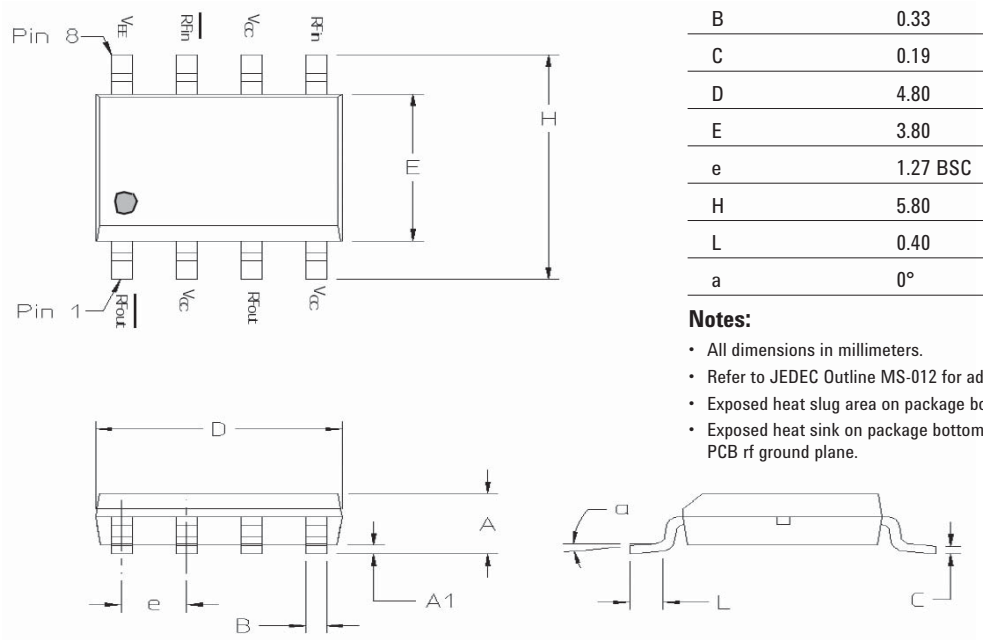
MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Moisture Sensitivity Classification: Class 1, per JESD22-A112-A.

Additional References:

PN #18, "HBT Prescaler Evaluation Board."



Symbol	Min.	Max.
A	1.35	1.75
A1	0.0	.25
B	0.33	0.51
C	0.19	.025
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	1.27 BSC
H	5.80	6.20
L	0.40	1.27
a	0°	8°

Notes:

- All dimensions in millimeters.
- Refer to JEDEC Outline MS-012 for additional tolerances.
- Exposed heat slug area on package bottom = 2.67 x 1.65.
- Exposed heat sink on package bottom must be soldered to PCB rf ground plane.

Figure 2. Package and dimensions

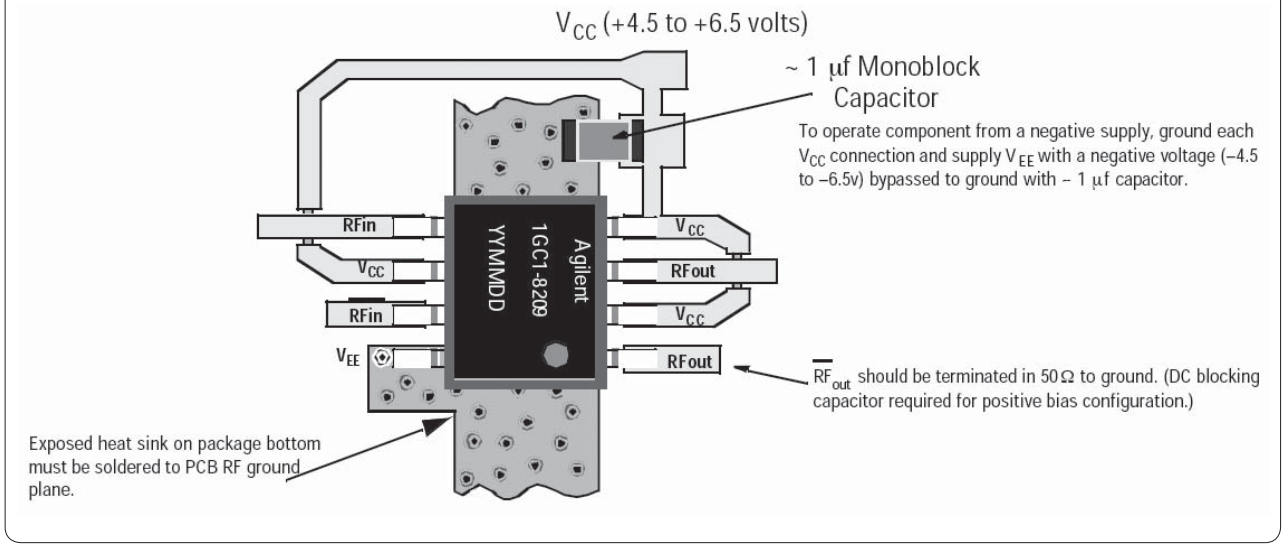


Figure 3. Assembly diagram (Single-supply, positive-bias configuration shown)

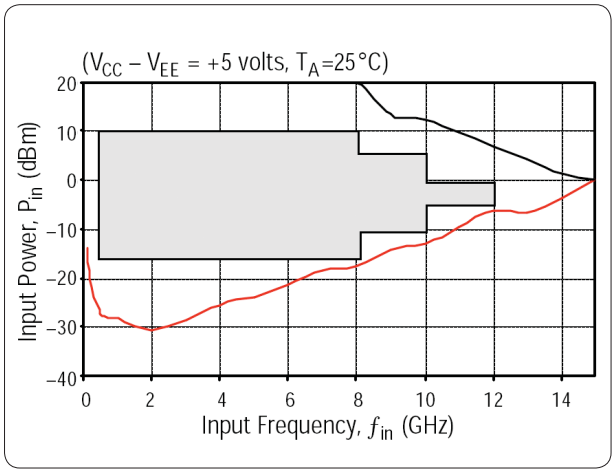


Figure 4. Typical input sensitivity window

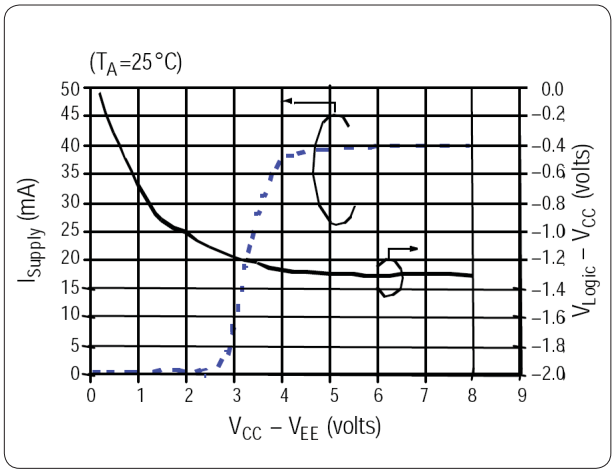


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

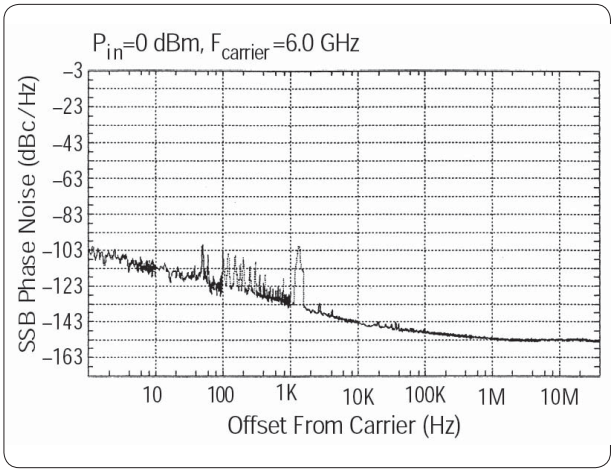


Figure 6. Typical phase noise performance

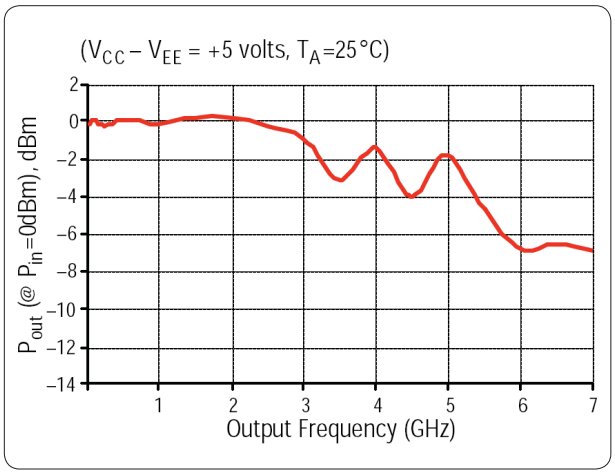


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

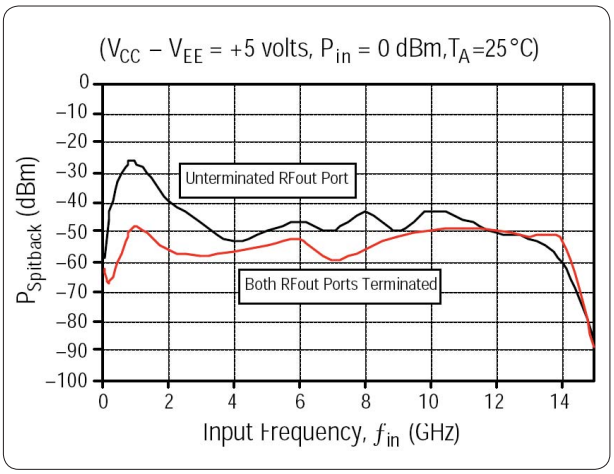
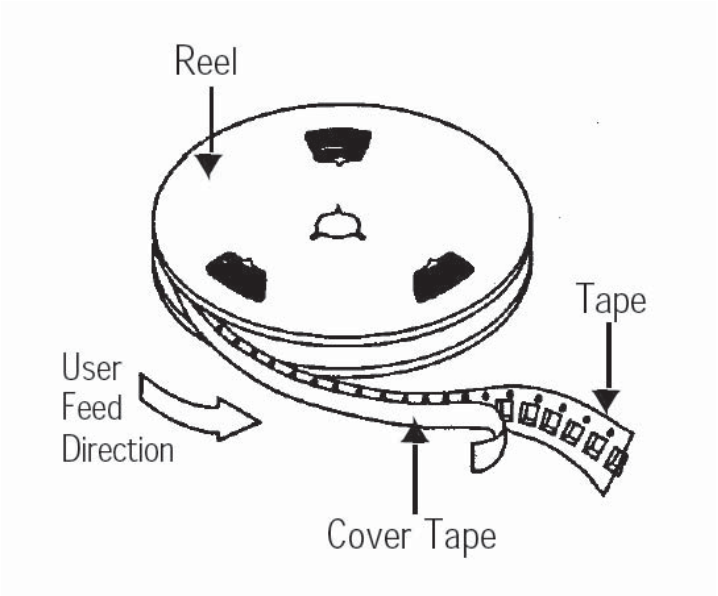
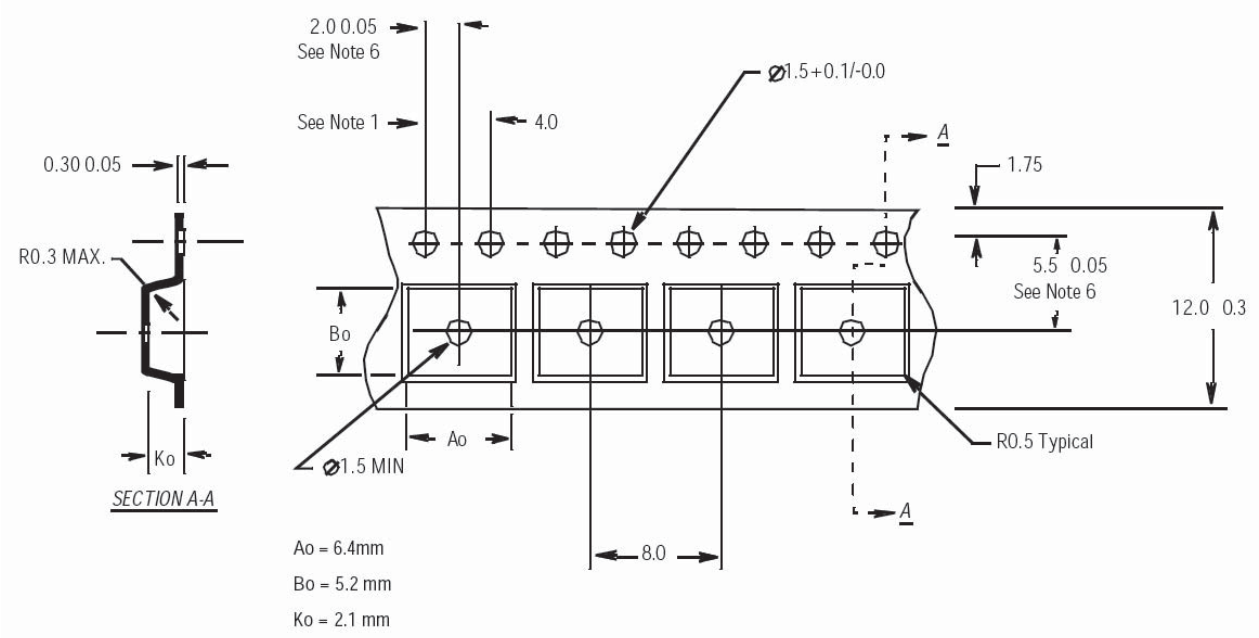


Figure 8. Typical "Spitback" power P(f_{out}) appearing at RF input port

Device Orientation



Tape Dimensions and Product Orientation



Notes:

1. 10 sprocket hole pitch cumulative tolerance: 0.2 mm.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3 mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

LXI

www.lxistandard.org
LXI is the LAN-based successor to GPIB, providing faster, more efficient connectivity. Agilent is a founding member of the LXI consortium.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifi cations. Customers considering the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifi cations from Agilent. In this data sheet the term typical refers to the 50th percentile performance. For additional information contact Agilent

MMIC_Helpline@agilent.com.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus
Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

Printed in USA, November 26, 2007
5989-7352EN

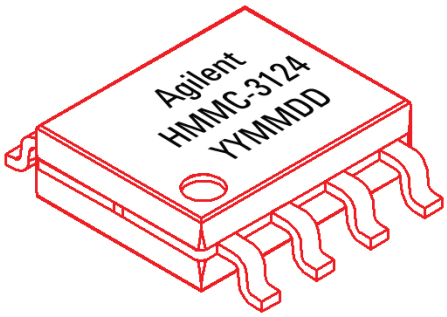
Agilent Technologies

Agilent HMMC-3124 DC-12 GHz Packaged High Efficiency Divide-by-4 Prescaler

1GC1-8207-TR1-7" diameter reel/500 each

1GC1-8207-BLK-bubble strip/10 each

Data Sheet



Package Type: 8-lead SOIC Plastic
Package Dimensions: 4.9 x 3.9 mm typ.
Package Thickness: 1.55 mm typ.
Lead Pitch: 1.25 mm nom.
Lead Width: 0.42 mm nom.

Features

- **Wide Frequency Range: 0.2-12 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -15 to +10 dBm (1-8 GHz) -10 to +8 dBm (8-10 GHz) -5 to +2 dBm (10-12 GHz)**
- **P_{out}: 0 dBm (0.5 V_{p-p})**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range: 4.5 to 6.5 volt operating range**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-3124 is a packaged GaAs HBT MMIC prescaler which offers dc to 12 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ $T_{BS} \leq 85°C$. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

DC Specifications/Physical Properties

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current	34	40	46	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.32	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	12	14		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self\text{-}Osc.}$	Output Self-Oscillation Frequency[2]		3.4		GHz
P_{in}	@ dc, (Square-wave input)	-15	> -25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	> -20	+10	dBm
	f_{in} = 1 to 8 GHz	-15	> -20	+10	dBm
	f_{in} = 8 to 10 GHz	-10	> -15	+5	dBm
	f_{in} = 10 to 12 GHz	-5	> -10	+1	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 10 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 10 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero-crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output transition time (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave input signal. Prescaler will operate down to dc for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Input dc offset technique described on page 4.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
P_{out}[3]	@ f_{out} < 1 GHz	-2	0		dBm
	@ f_{out} = 2.5 GHz	-3.5	-1.5		dBm
	@ f_{out} = 3.0 GHz	-4.5	-2.5		dBm
$\lvert V_{out(p-p)} \rvert$[4]	@ f_{out} < 1 GHz		0.5		volts
	@ f_{out} = 2.5 GHz		0.42		volts
	@ f_{out} = 3.0 GHz		0.37		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 10 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-50		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-55		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in}))		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out} (f_{out}))		-25		dBc

Notes

3. Fundamental of output square wave's Fourier Series.
4. Square wave amplitude calculated from P_{out}.

Applications

The HMMC-3124 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 12 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

Due to the presence of an off-chip RF-bypass capacitor inside the package (connected to the V_{CC} contact on the device), and the unique design of the device itself, the component may be biased from either a single positive or single negative supply bias. The backside of the package is not dc connected to any dc bias point on the device.

For positive supply operation, V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with pin 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to pin 8 (V_{EE}).

AC-Coupling and DC-Blocking

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not dc grounded the RF ports should be ac coupled via series capacitors mounted on the PC board at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the package heat sink may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

Input DC Offset

If an RF signal with sufficient signal to noise ratio is present at the RF input lead, the prescaler will operate and provide a divided output equal the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the component may "self-oscillate", especially under small signal input powers or with only noise present at the input. This "self-oscillation" will produce a undesired output signal also known as a false trigger. To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV dc offset voltage between the RF_{in} and $\overline{RF_{in}}$ ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 kΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ≈ 25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

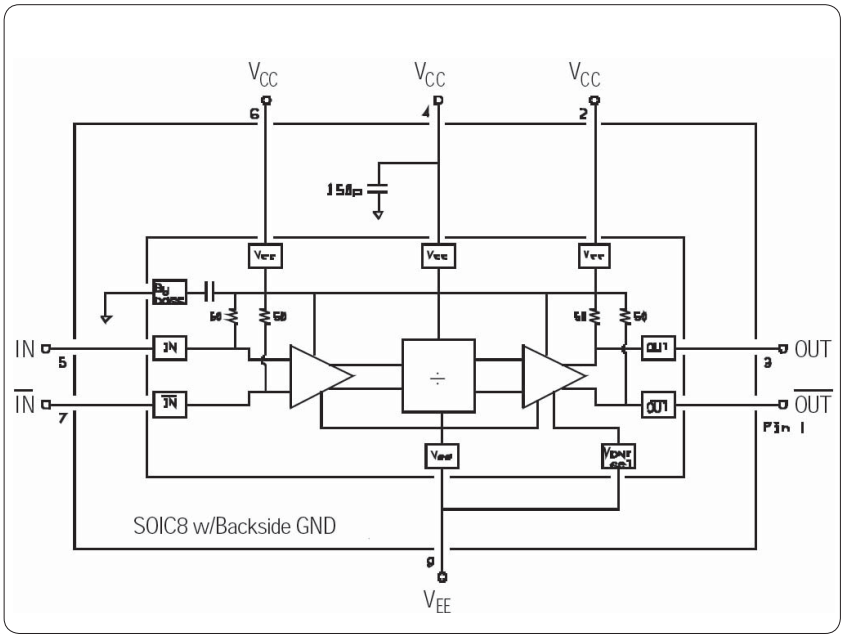


Figure 1. Simplified Schematic

Assembly Notes

Independent of the bias applied to the package, the backside of the package should always be connected to both a good RF ground plane and a good thermal heat sinking region on the PC board to optimize performance. For single-ended output operation the unused RF output lead should be terminated into 50 Ω to a contact point at the V_{CC} potential or to RF ground through a dc blocking capacitor.

A minimum RF and thermal PC board contact area equal to or greater than 2.67 × 1.65 mm (0.105" × 0.065") with eight 0.020" diameter plated-wall thermal vias is recommended.

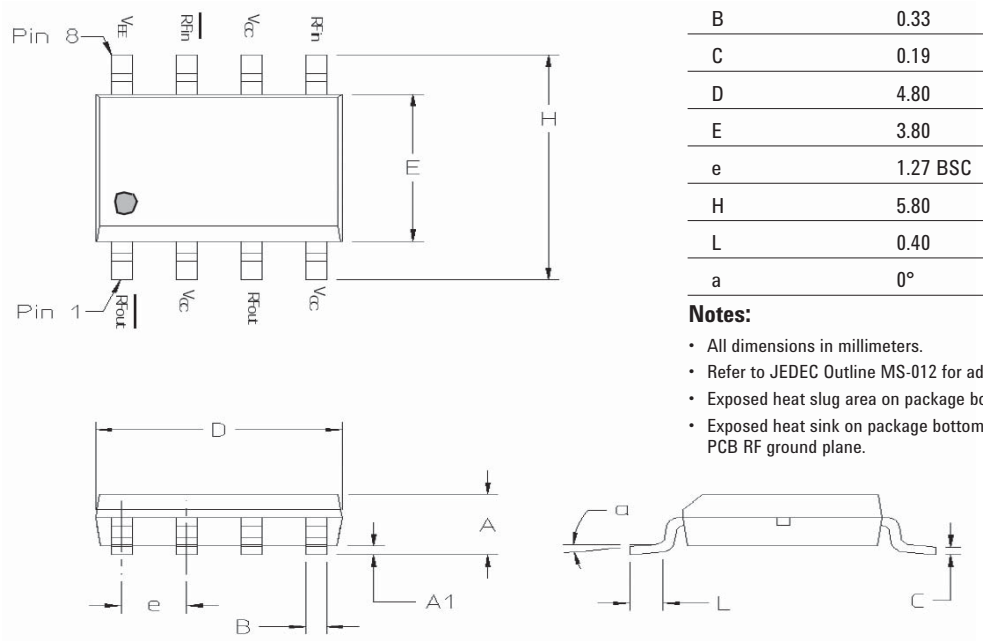
MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Moisture Sensitivity Classification: Class 1, per JESD22-A112-A.

Additional References:

PN #18, "HBT Prescaler Evaluation Board."



Symbol	Min.	Max.
A	1.35	1.75
A1	0.0	.25
B	0.33	0.51
C	0.19	.025
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	1.27 BSC
H	5.80	6.20
L	0.40	1.27
a	0°	8°

Notes:

- All dimensions in millimeters.
- Refer to JEDEC Outline MS-012 for additional tolerances.
- Exposed heat slug area on package bottom = 2.67 x 1.65.
- Exposed heat sink on package bottom must be soldered to PCB RF ground plane.

Figure 2. Package and dimensions

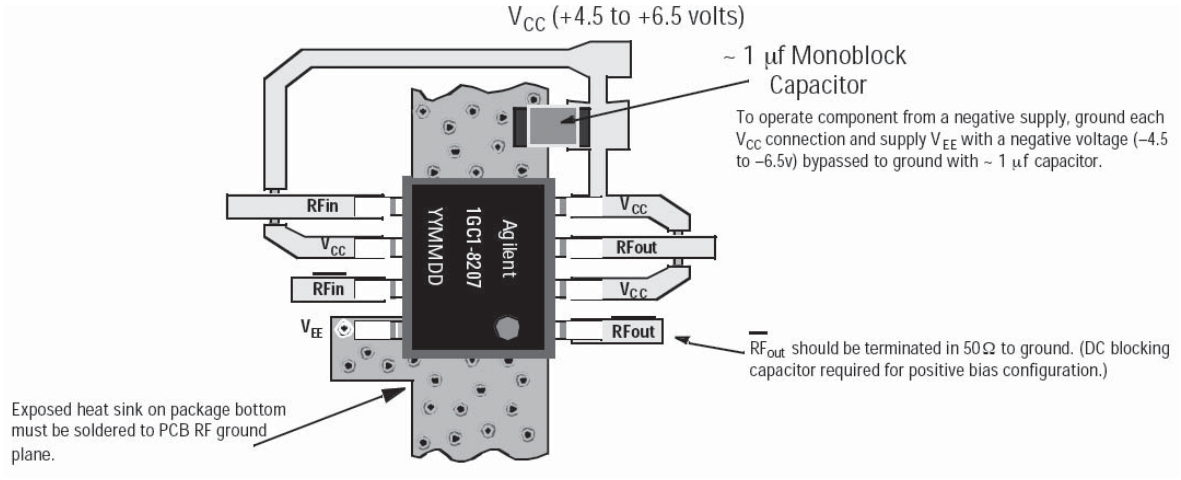


Figure 3. Assembly diagram (Single-supply, positive-bias configuration shown)

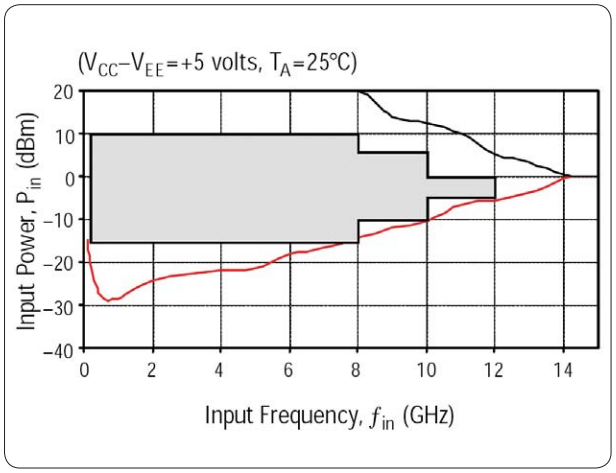


Figure 4. Typical input sensitivity window

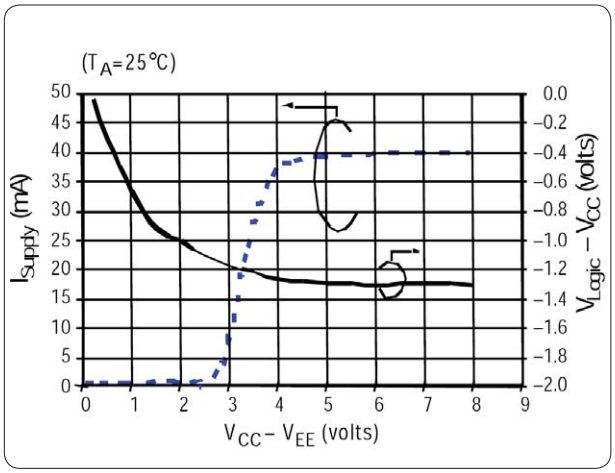


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

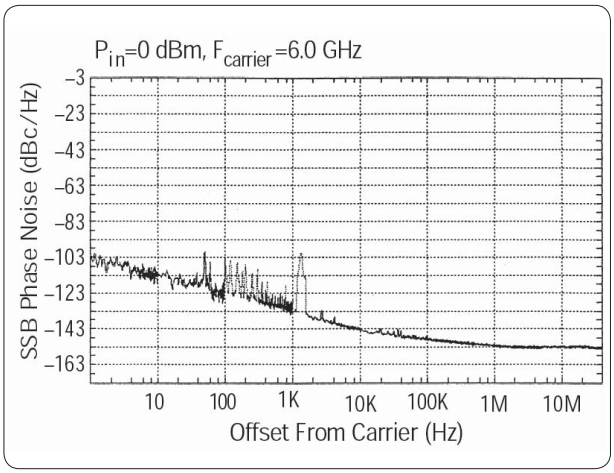


Figure 6. Typical phase noise performance

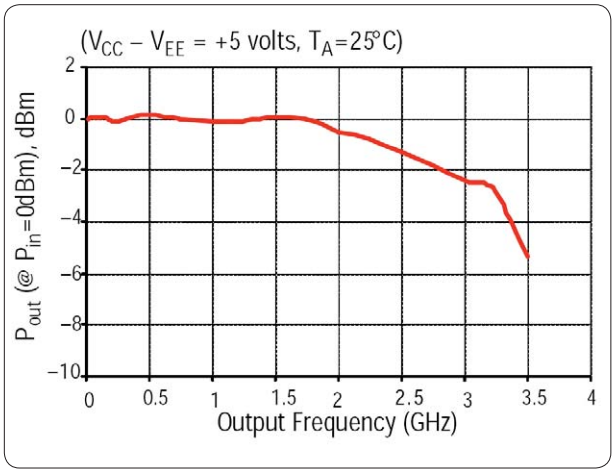


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

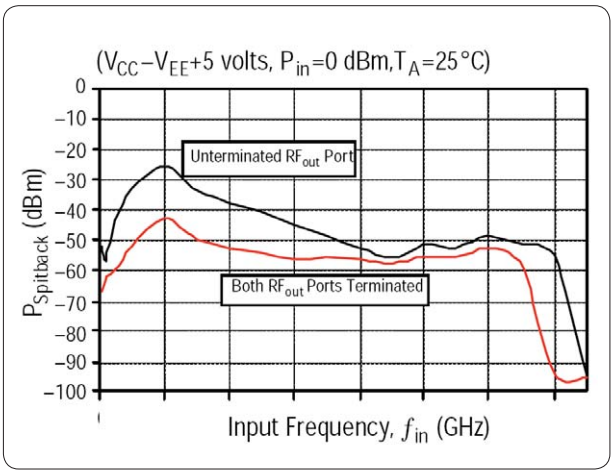
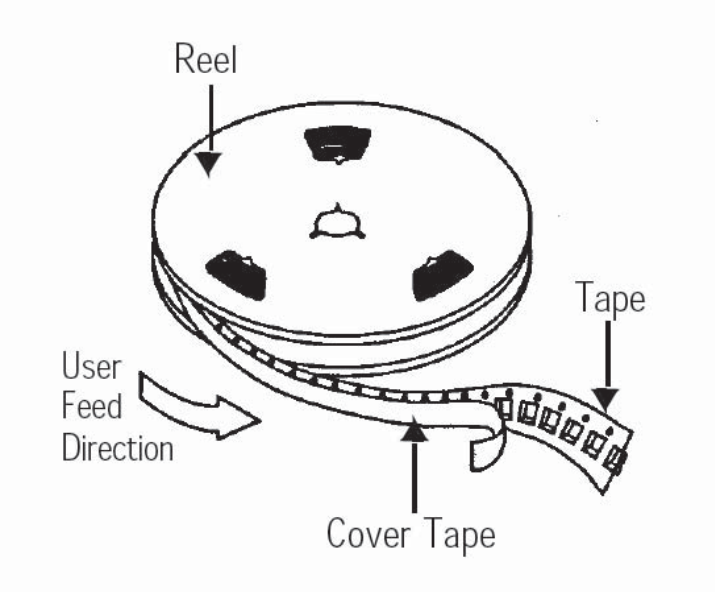
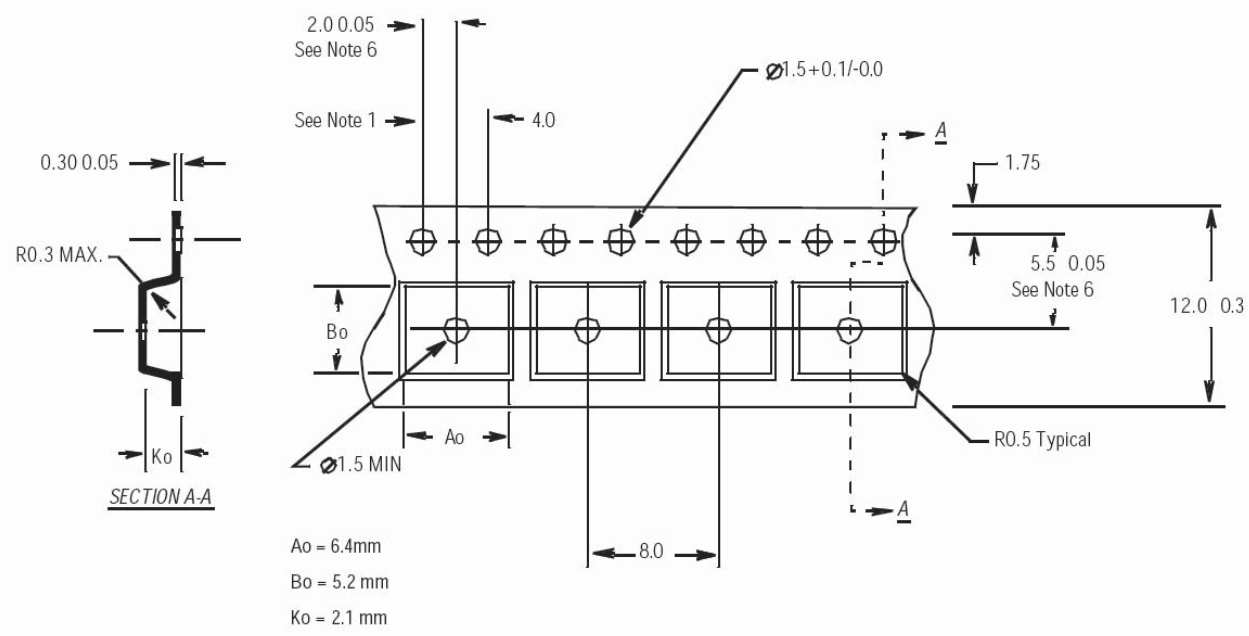


Figure 8. Typical "Spitback" power P(f_{out}) appearing at RF input port

Device Orientation



Tape Dimensions and Product Orientation



Notes:

1. 10 sprocket hole pitch cumulative tolerance: 0.2 mm.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3 mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

LXI

www.lxistandard.org
LXI is the LAN-based successor to GPIB, providing faster, more efficient connectivity. Agilent is a founding member of the LXI consortium.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifi cations. Customers considering the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifi cations from Agilent. In this data sheet the term typical refers to the 50th percentile performance. For additional information contact Agilent

MMIC_Helpline@agilent.com.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus
Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

Printed in USA, November 26, 2007
5989-7353EN

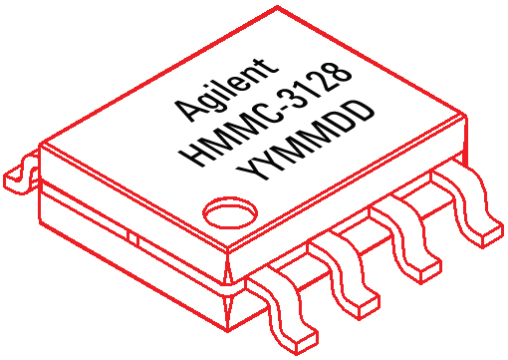
Agilent Technologies

Agilent HMMC-3128 DC-12 GHz Packaged High Efficiency Divide-by-8 Prescaler

1GC1-8208-TR1-7" diameter reel/500 each

1GC1-8208-BLK-bubble strip/10 each

Data Sheet



Features

- **Wide Frequency Range: 0.2-12 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -15 to +10 dBm (1- 8 GHz) -10 to +8 dBm (8-10 GHz) -5 to +2 dBm (10-12 GHz)**
- **P_{out}: 0 dBm (0.5 V_{p-p})**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range: 4.5 to 6.5 volt operating range**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-3128 is a packaged GaAs HBT MMIC pre-scaler which offers dc to 12 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.

Package Type:	8-lead SOIC Plastic
Package Dimensions:	4.9 x 3.9 mm typ.
Package Thickness:	1.55 mm typ.
Lead Pitch:	1.25 mm nom.
Lead Width:	0.42 mm nom.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ $T_{BS} \leq 85°C$. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

DC Specifications/Physical Properties

(T_A = 25°C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current	37	44	51	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.32	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	12	14		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self\text{-}Osc.}$	Output Self-Oscillation Frequency[2]		3.4		GHz
P_{in}	@ dc, (Square-wave input)	-15	> -25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	> -20	+10	dBm
	f_{in} = 1 to 8 GHz	-15	> -20	+10	dBm
	f_{in} = 8 to 10 GHz	-10	> -15	+5	dBm
	f_{in} = 10 to 12 GHz	-5	> -10	-1	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 10 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 10 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero-crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output transition time (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave input signal. Prescaler will operate down to dc for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Input dc offset technique described on page 4.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
P_{out}[3]	@ f_{out} < 1 GHz	-2	0		dBm
	@ f_{out} = 2.5 GHz	-3.5	-1.5		dBm
	@ f_{out} = 3.0 GHz	-4.5	-2.5		dBm
$\lvert V_{out(p-p)} \rvert$[4]	@ f_{out} < 1 GHz		0.5		volts
	@ f_{out} = 2.5 GHz		0.42		volts
	@ f_{out} = 3.0 GHz		0.37		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 10 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-50		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-55		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in}))		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out} (f_{out}))		-25		dBc

Notes

3. Fundamental of output square wave's Fourier Series.
4. Square wave amplitude calculated from P_{out}.

Applications

The HMMC-3128 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 12 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

Due to the presence of an off-chip RF-bypass capacitor inside the package (connected to the V_{CC} contact on the device), and the unique design of the device itself, the component may be biased from either a single positive or single negative supply bias. The backside of the package is not dc connected to any dc bias point on the device.

For positive supply operation, V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with pin 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to pin 8 (V_{EE}).

AC-Coupling and DC-Blocking

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not dc grounded the RF ports should be ac coupled via series capacitors mounted on the PC board at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the package heat sink may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

Input DC Offset

If an RF signal with sufficient signal to noise ratio is present at the RF input lead, the prescaler will operate and provide a divided output equal the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the component may “self-oscillate”, especially under small signal input powers or with only noise present at the input. This “self-oscillation” will produce a undesired output signal also known as a false trigger. To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV dc offset voltage between the RF_{in} and $\overline{RF}_{in}$ ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 kΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ≈ 25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

Assembly Notes

Independent of the bias applied to the package, the backside of the package should always be connected to both a good RF ground plane and a good thermal heat sinking region on the PC board to optimize performance. For single-ended output operation the unused RF output lead should be terminated into 50 Ω to a contact point at the V_{CC} potential or to RF ground through a dc blocking capacitor.

A minimum RF and thermal PC board contact area equal to or greater than 2.67 × 1.65 mm (0.105" × 0.065") with eight 0.020" diameter plated-wall thermal vias is recommended.

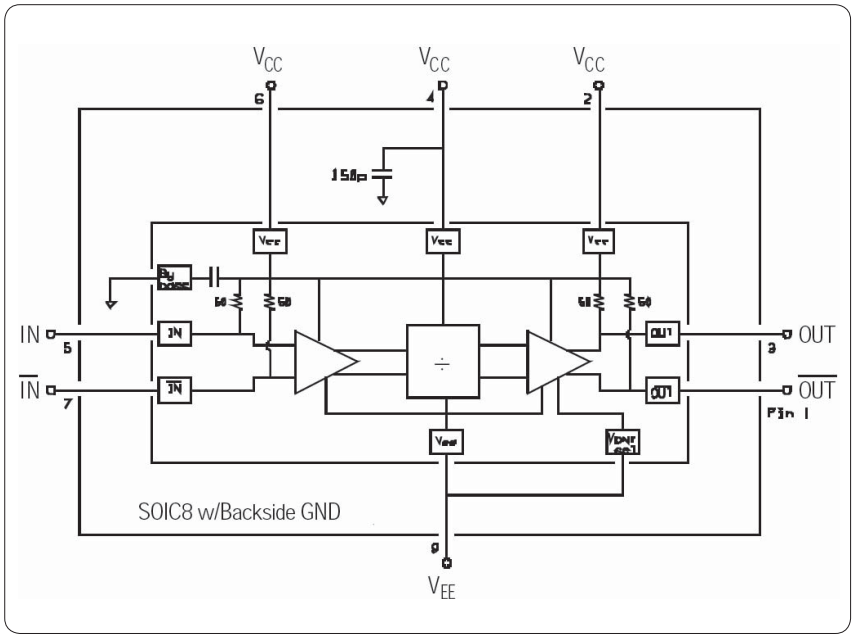


Figure 1. Simplified Schematic

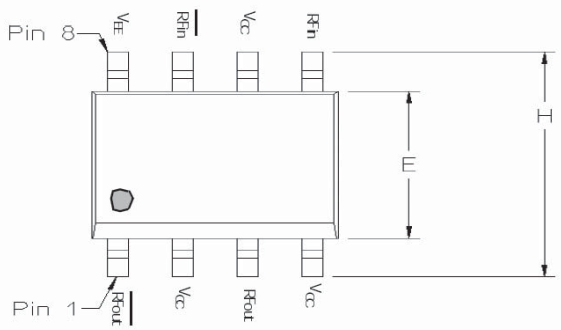
MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

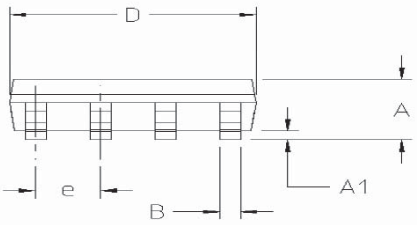
Agilent application note #54, “GaAs MMIC ESD, Die Attach and Bonding Guidelines” provides basic information on these subjects.

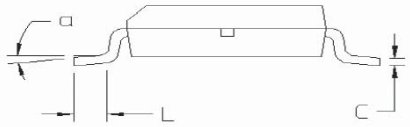
Moisture Sensitivity Classification: Class 1, per JESD22-A112-A.

Additional References:

PN #18, "HBT Prescaler Evaluation Board."







Symbol	Min.	Max.
A	1.35	1.75
A1	0.0	.25
B	0.33	0.51
C	0.19	.025
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	1.27 BSC
H	5.80	6.20
L	0.40	1.27
a	0°	8°

Notes:

- All dimensions in millimeters.
- Refer to JEDEC Outline MS-012 for additional tolerances.
- Exposed heat slug area on package bottom = 2.67 x 1.65.
- Exposed heat sink on package bottom must be soldered to PCB RF ground plane.

Figure 2. Package and dimensions

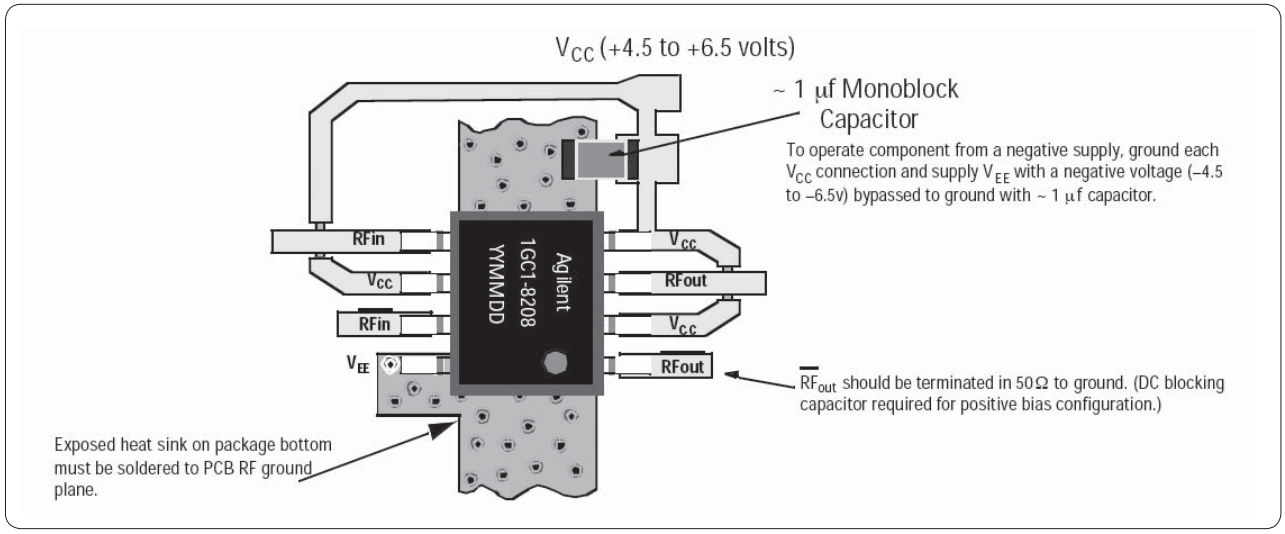


Figure 3. Assembly diagram (Single-supply, positive-bias configuration shown)

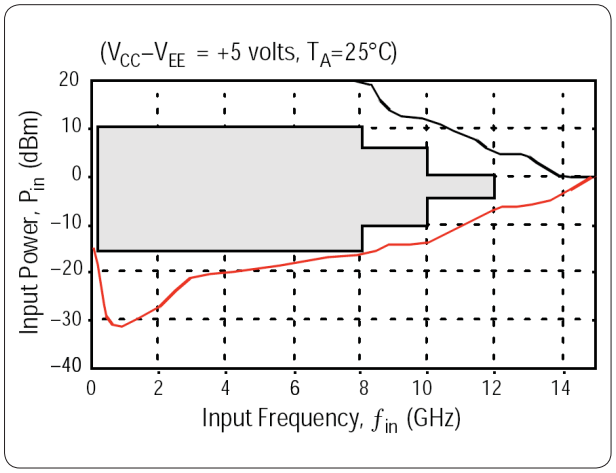


Figure 4. Typical input sensitivity window

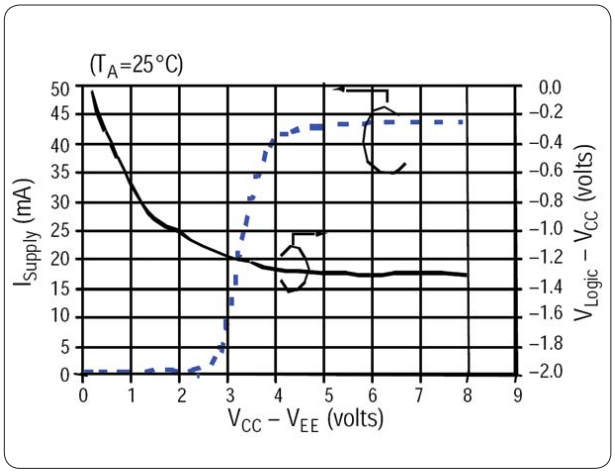


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

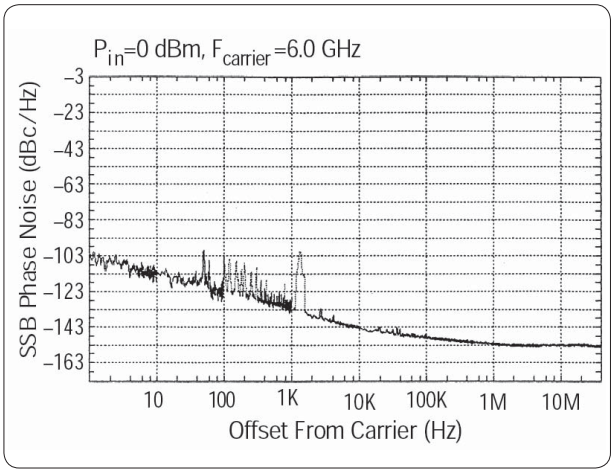


Figure 6. Typical phase noise performance

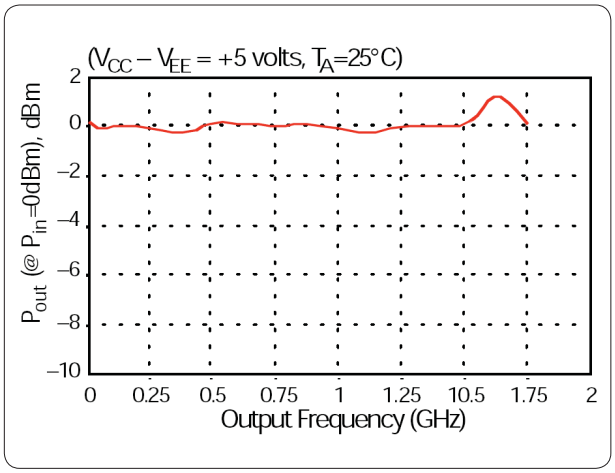


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

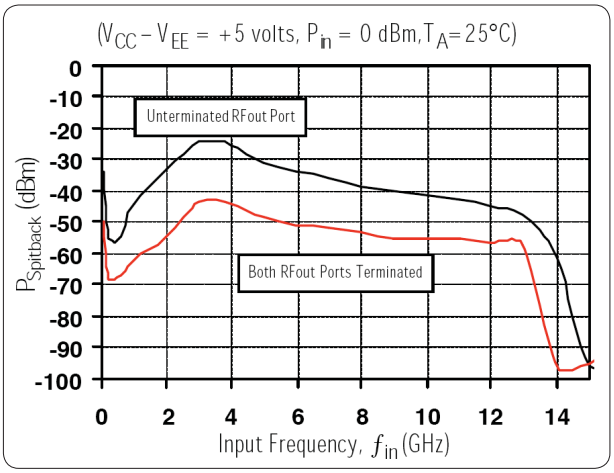
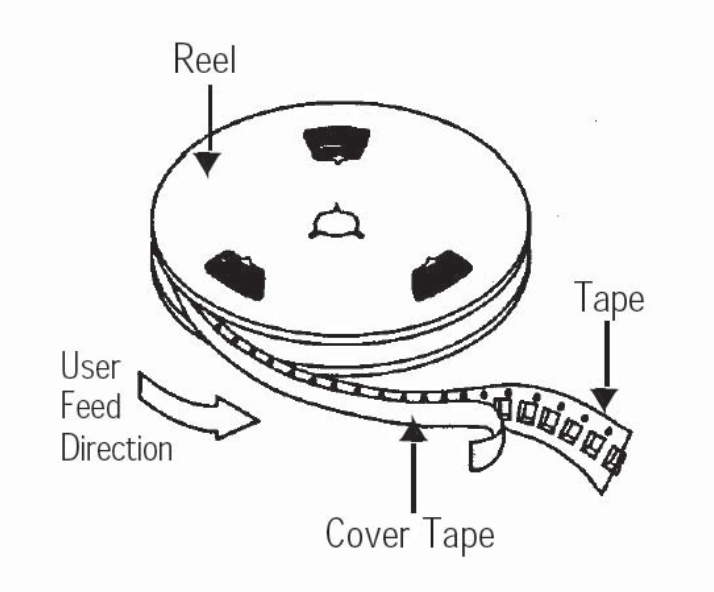
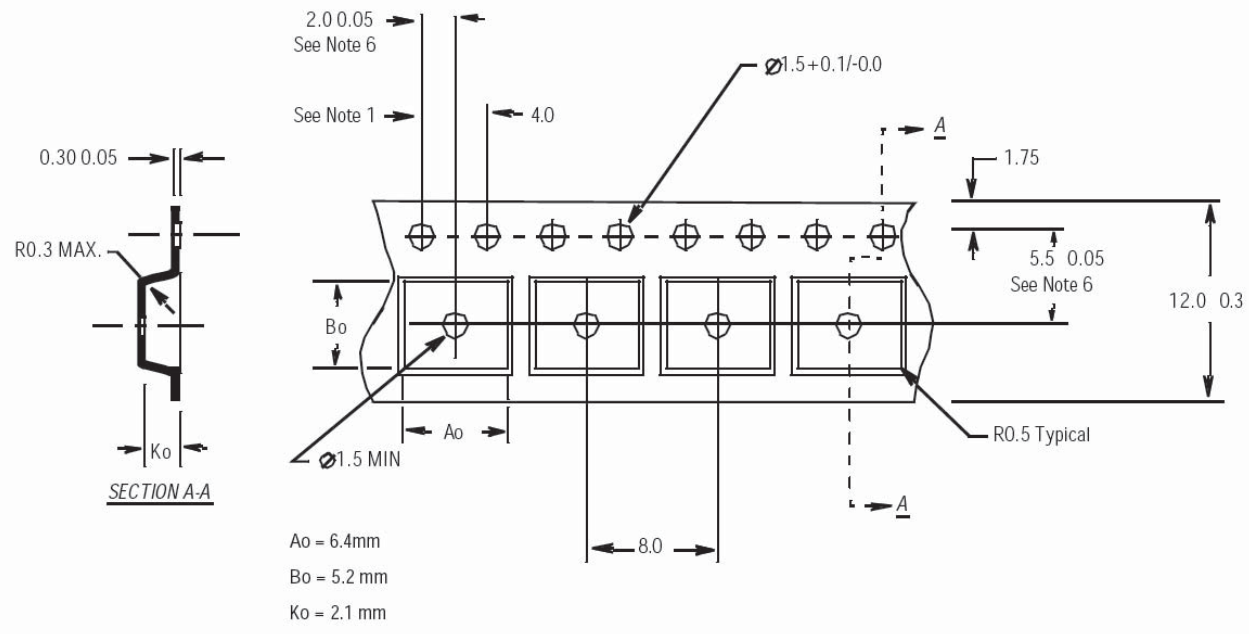


Figure 8. Typical "Spitback" power P(f_{out}) appearing at RF input port

Device Orientation



Tape Dimensions and Product Orientation



Notes:

1. 10 sprocket hole pitch cumulative tolerance: 0.2 mm.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3 mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

LXI

www.lxistandard.org
LXI is the LAN-based successor to GPIB, providing faster, more efficient connectivity. Agilent is a founding member of the LXI consortium.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifi cations. Customers considering the use of this, or other Agilent GaAs ICs, for their design should obtain the current production specifi cations from Agilent. In this data sheet the term typical refers to the 50th percentile performance. For additional information contact Agilent

MMIC_Helpline@agilent.com.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	81 426 56 7832
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700
Germany	01805 24 6333*
	*0.14 €/minute
Ireland	1890 924 204
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland (French)	41 (21) 8113811(Opt 2)
Switzerland (German)	0800 80 53 53 (Opt 1)
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus
Revised: May 7, 2007

Product specifications and descriptions in this document subject to change without notice.

Printed in USA, November 26, 2007
5989-7354EN

Agilent Technologies